

FIG. 1

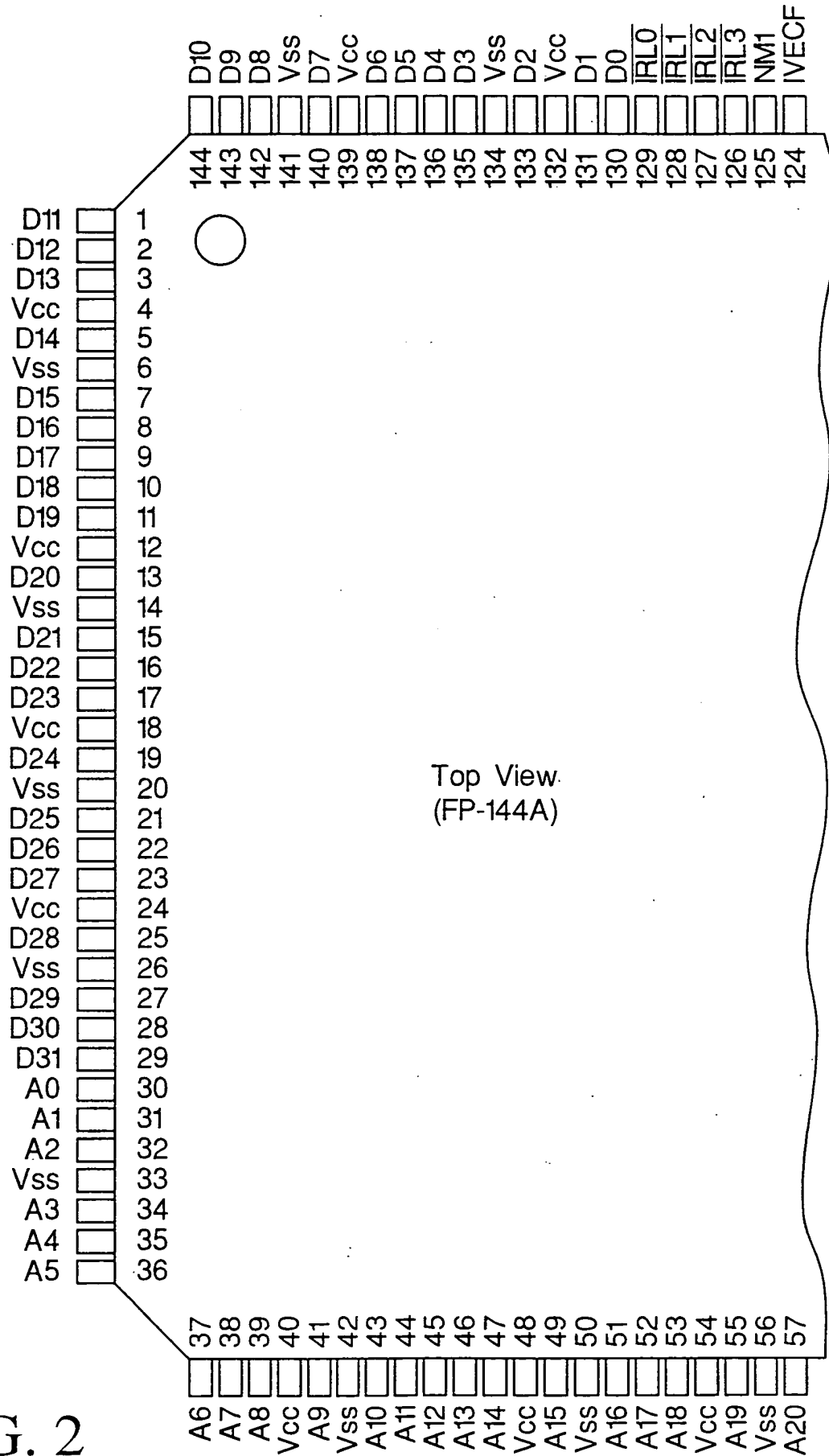


FIG. 2

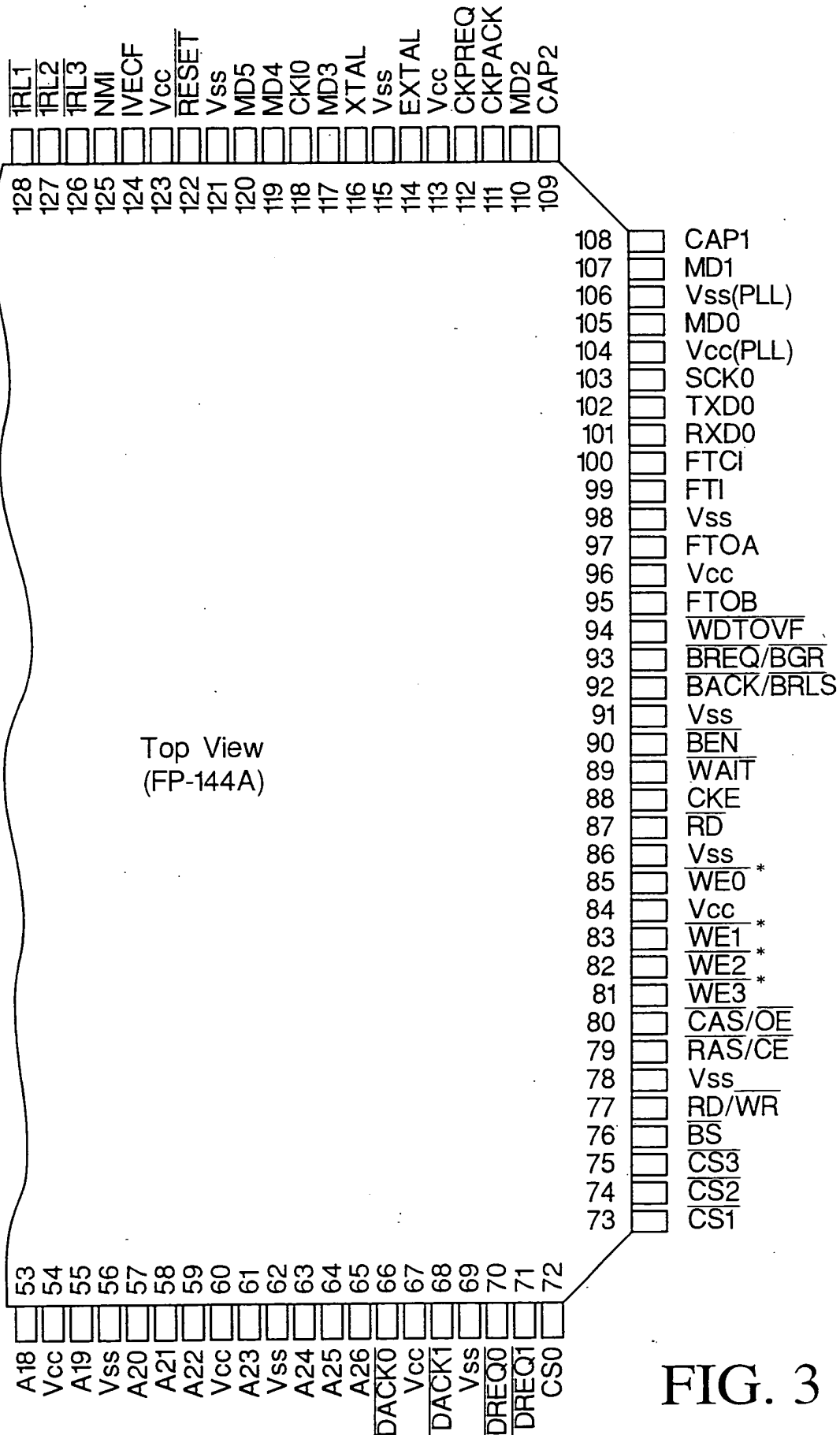


FIG. 3

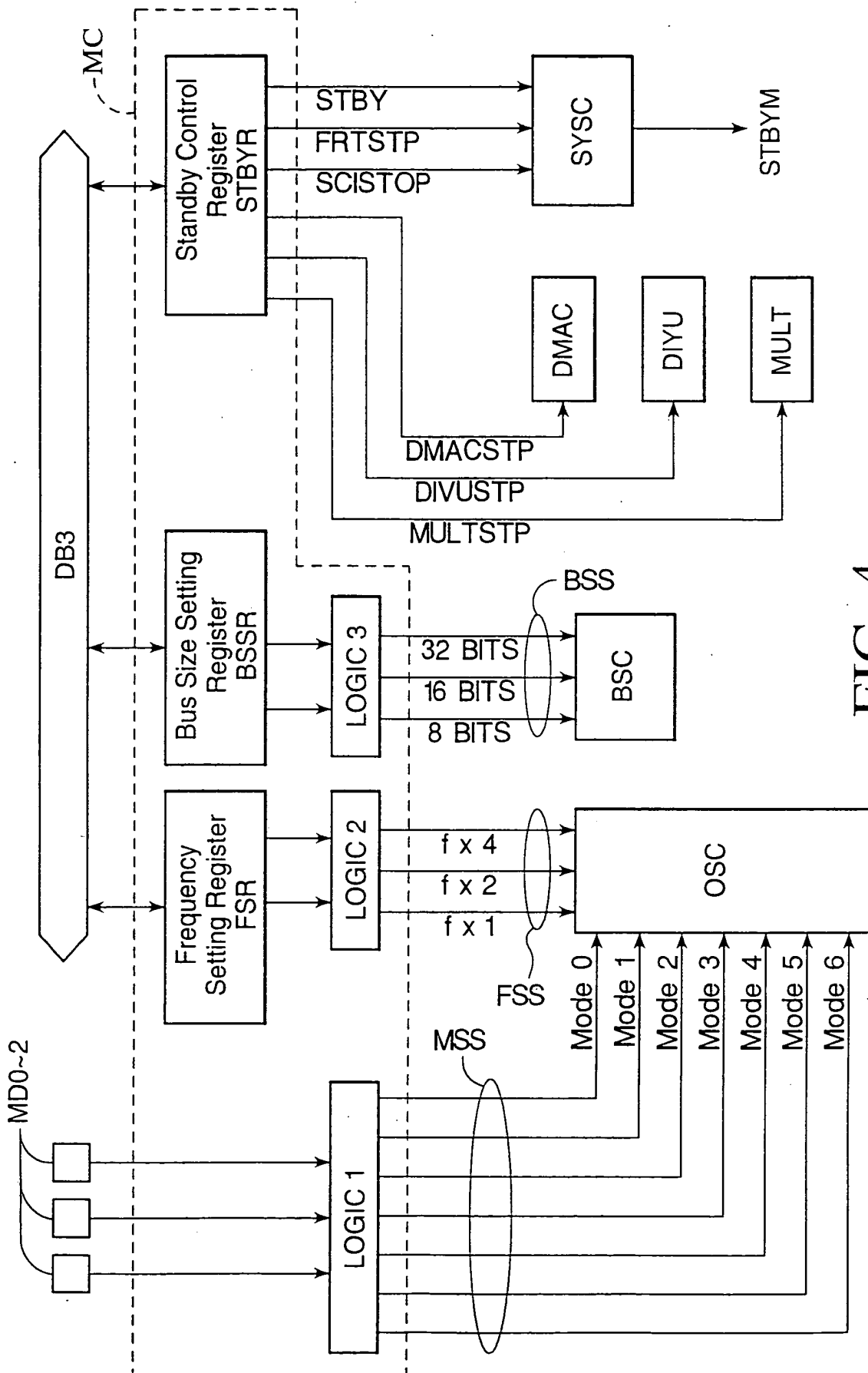


FIG. 4

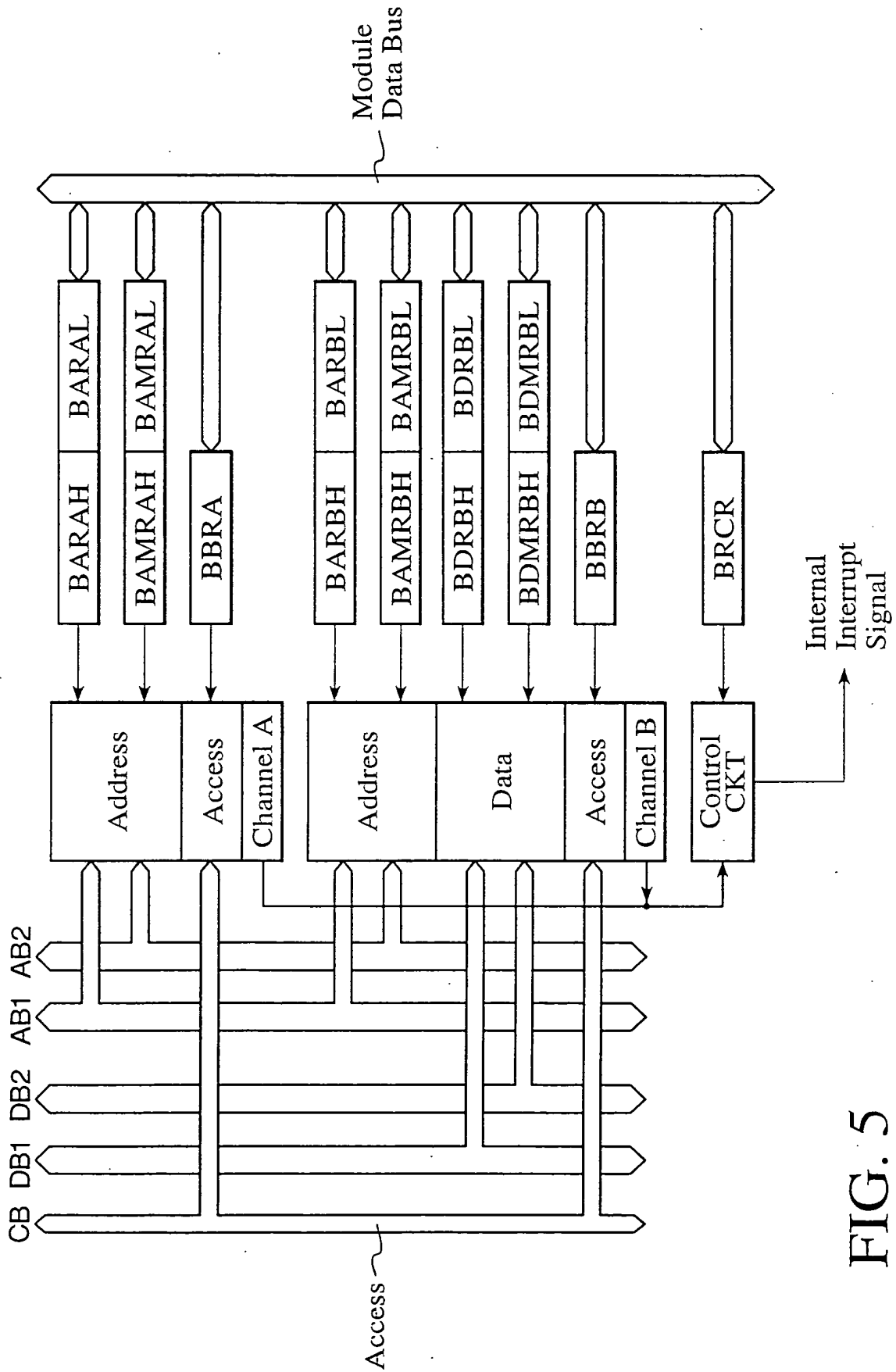
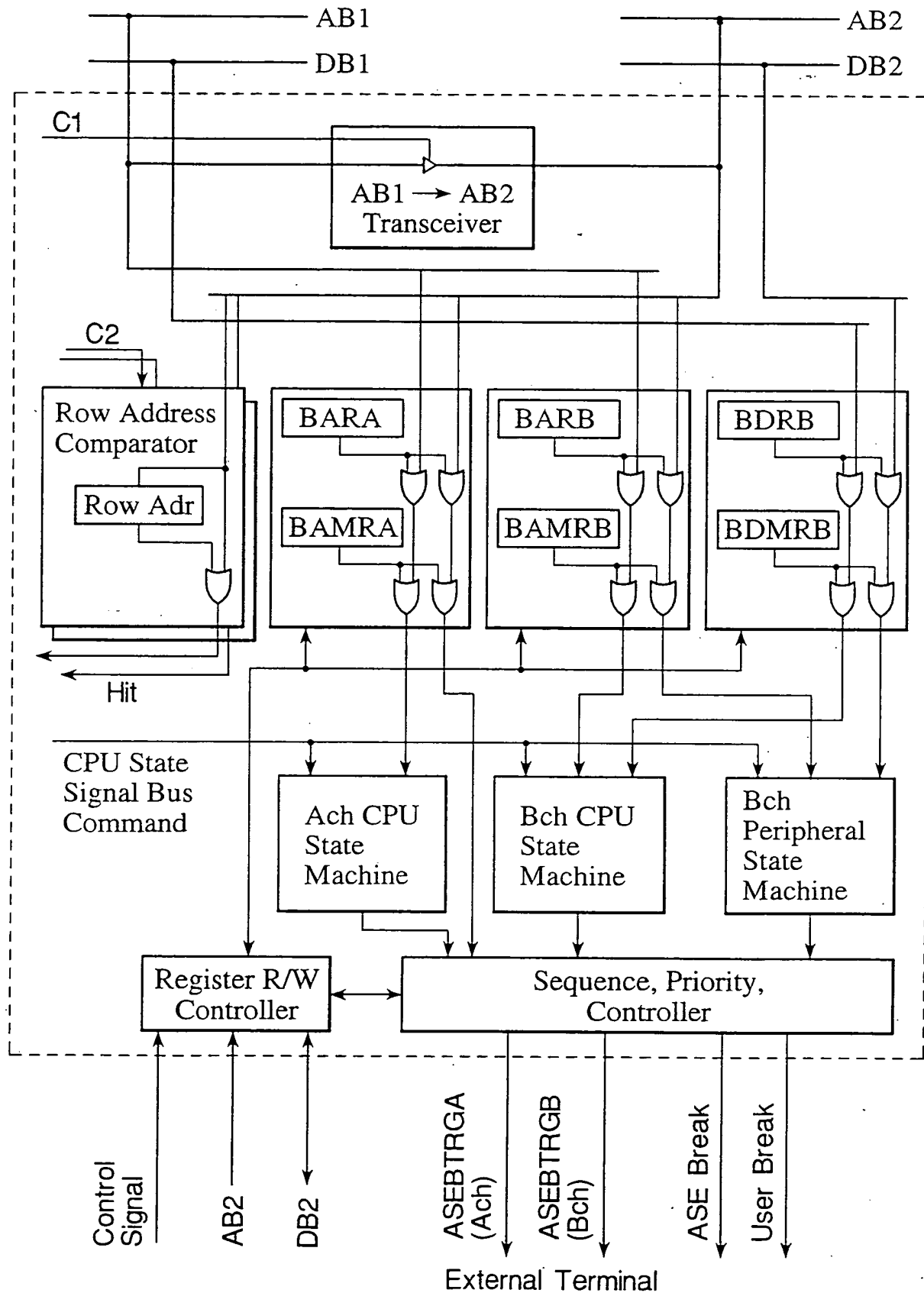


FIG. 5

FIG. 6



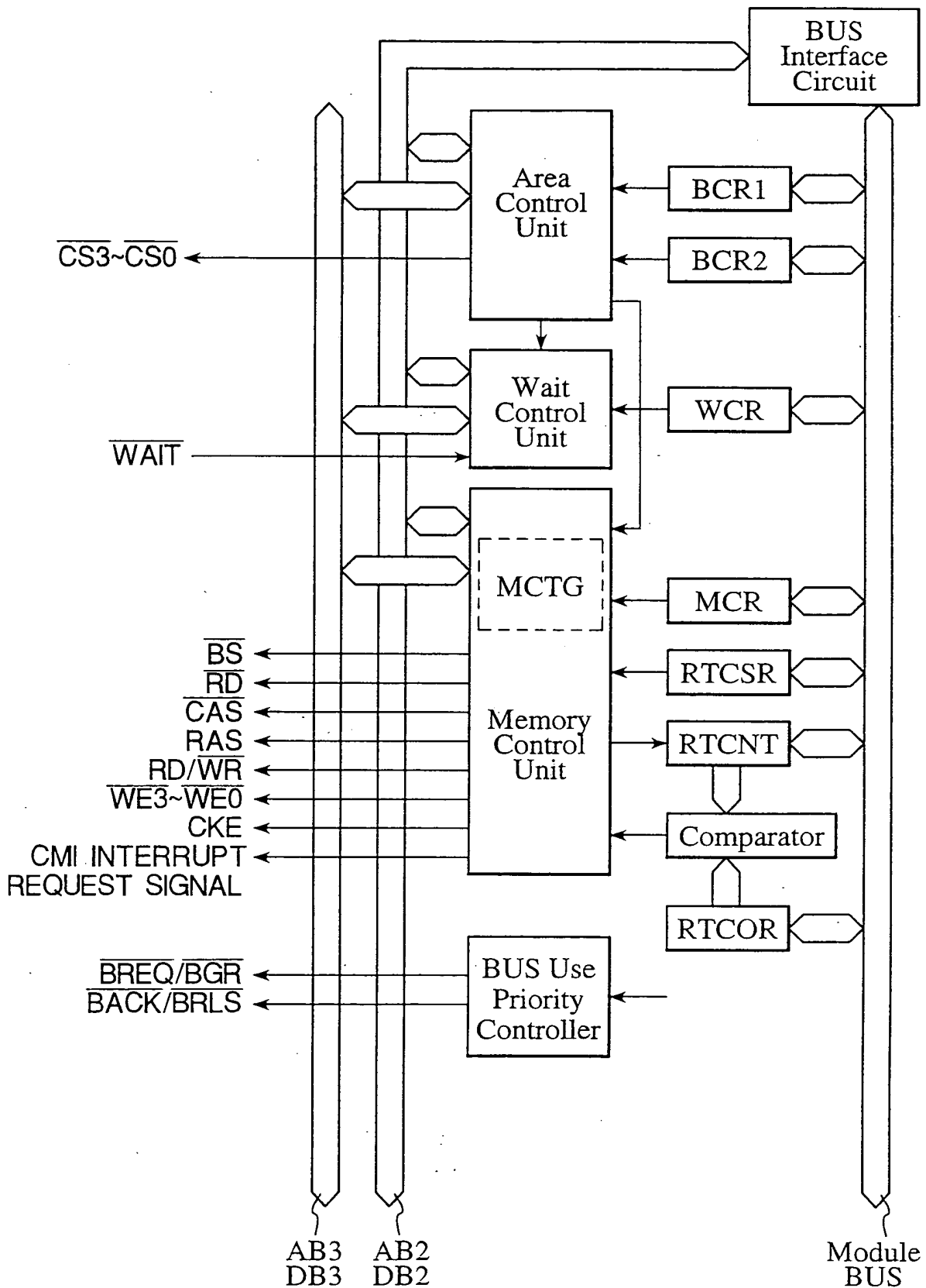


FIG. 7

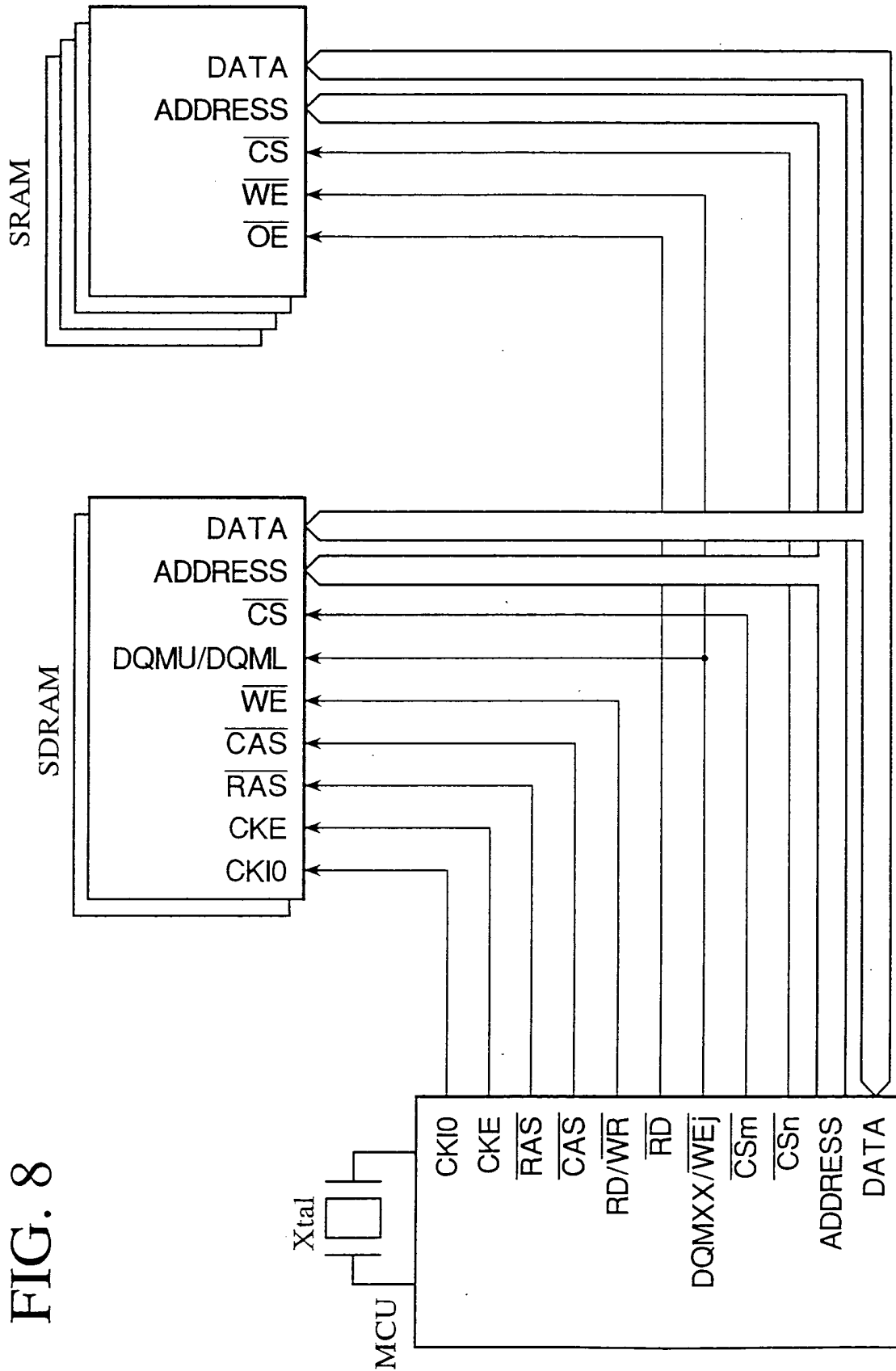


FIG. 8



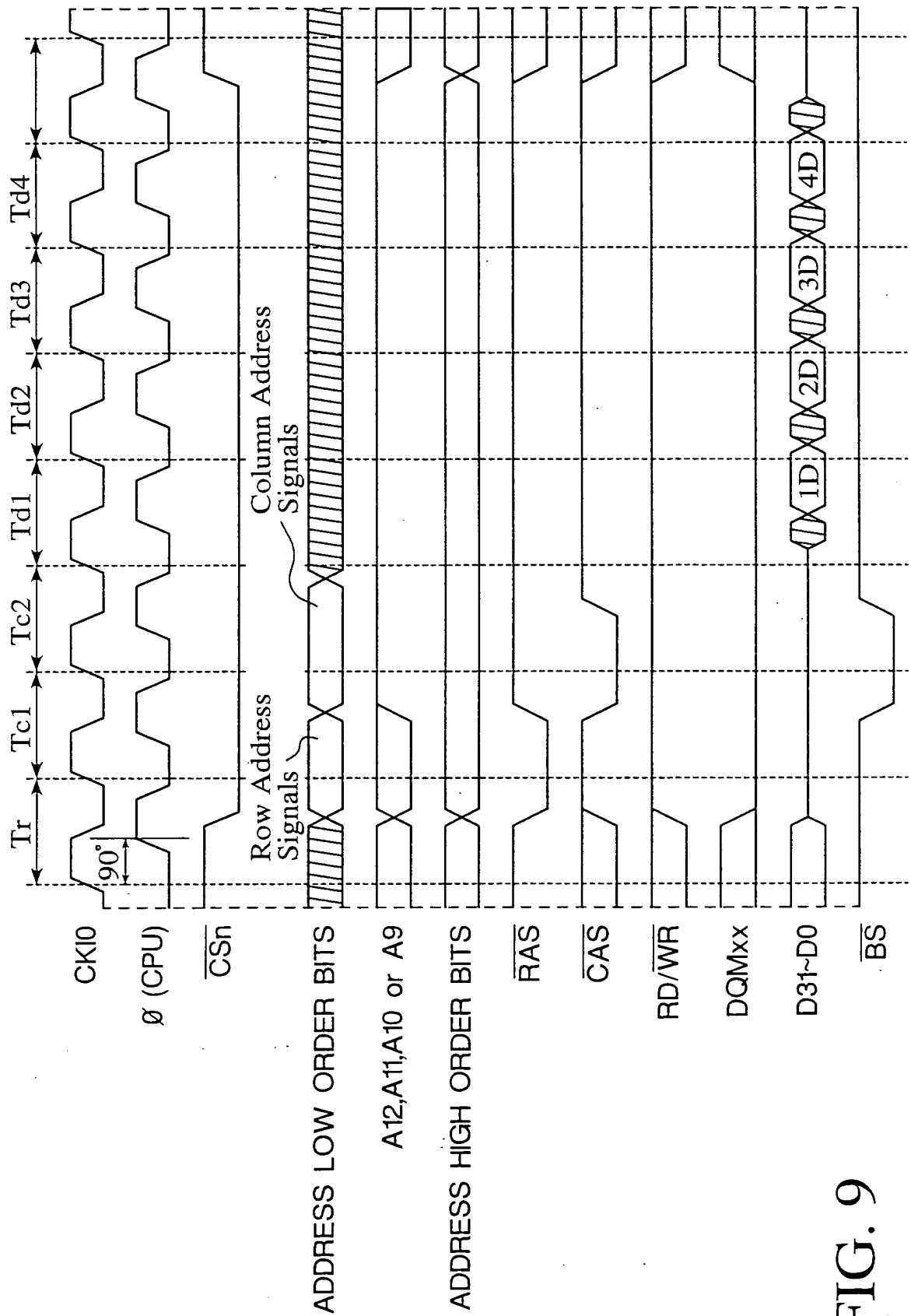


FIG. 9

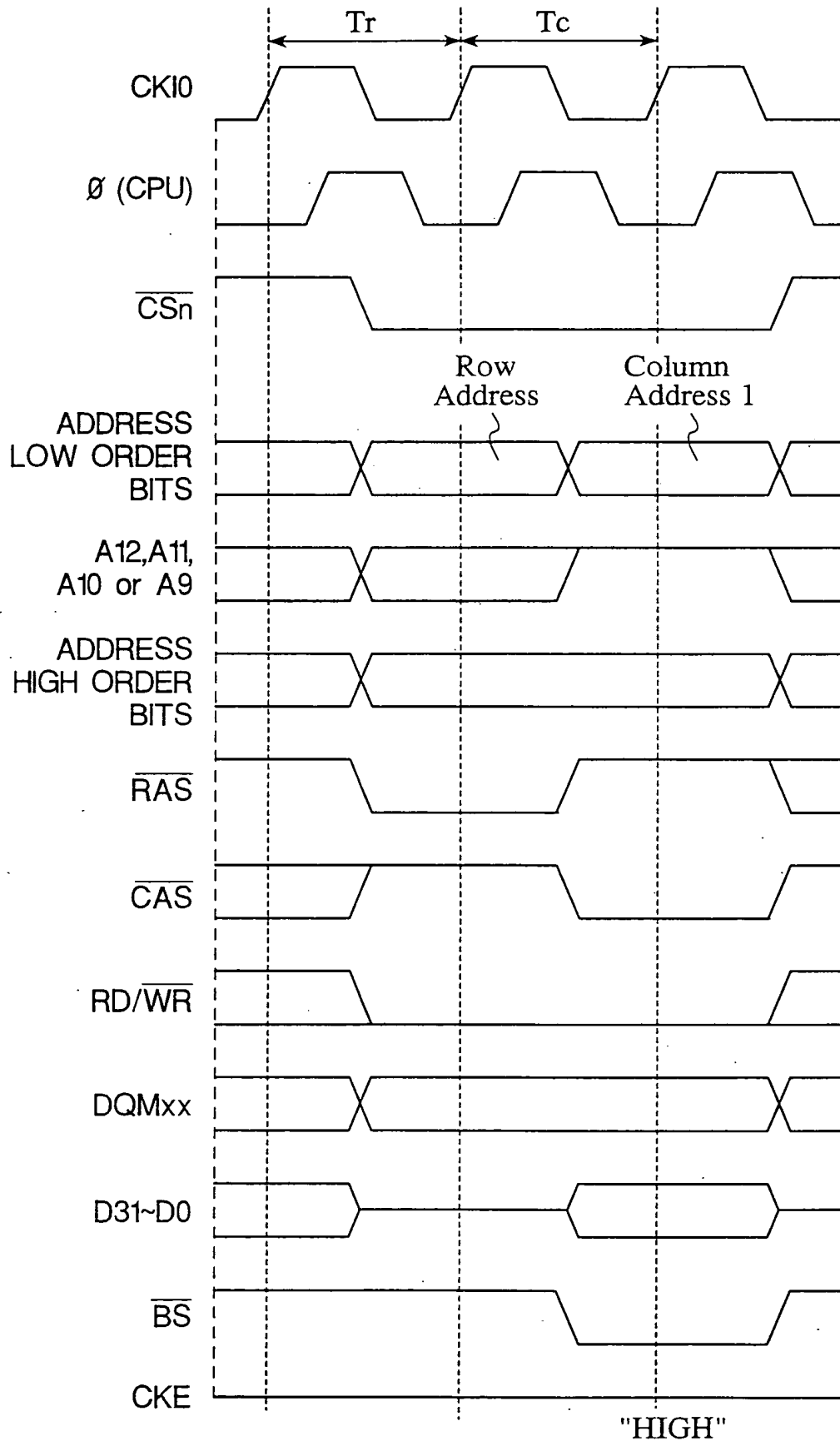


FIG. 10

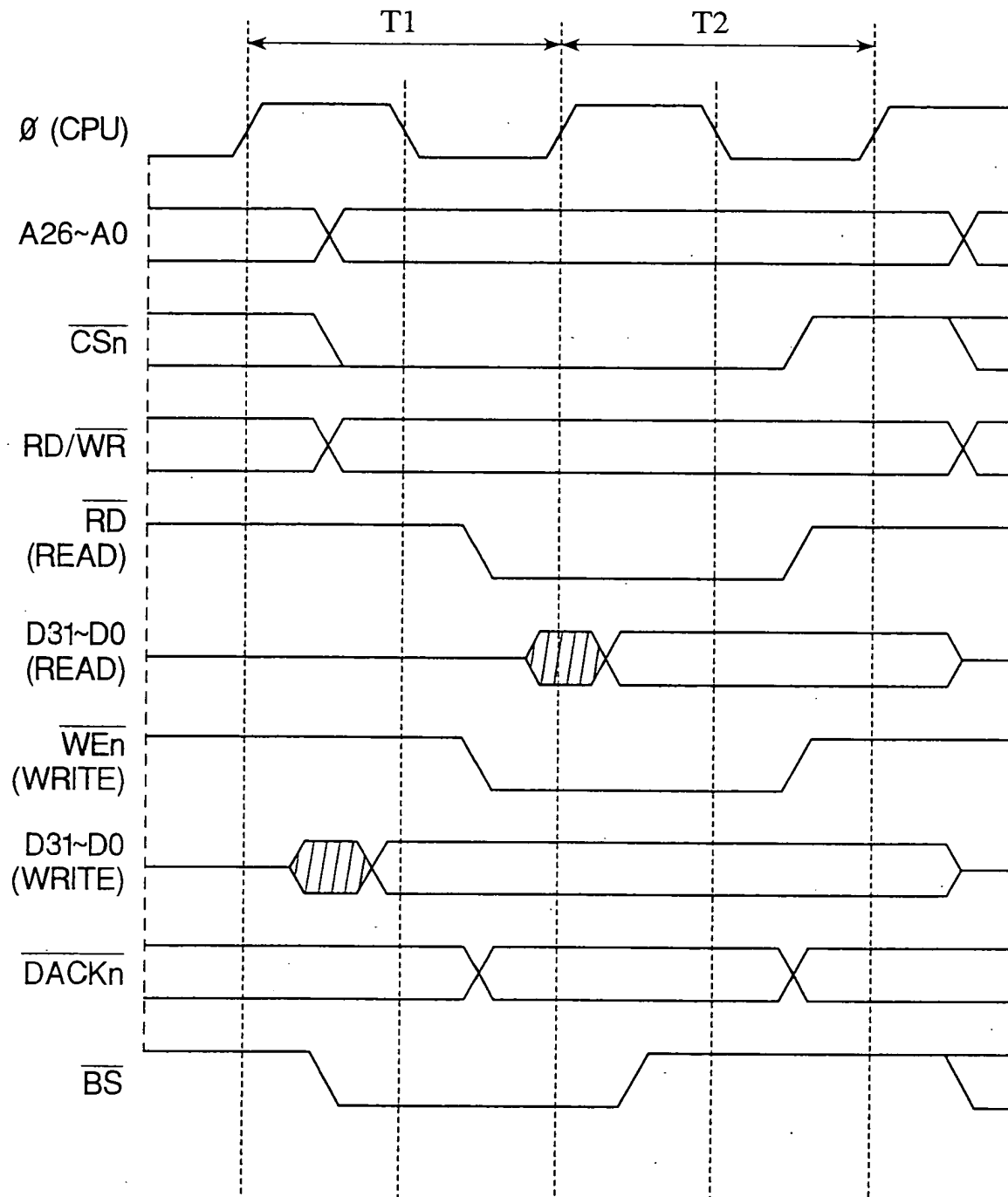


FIG. 11

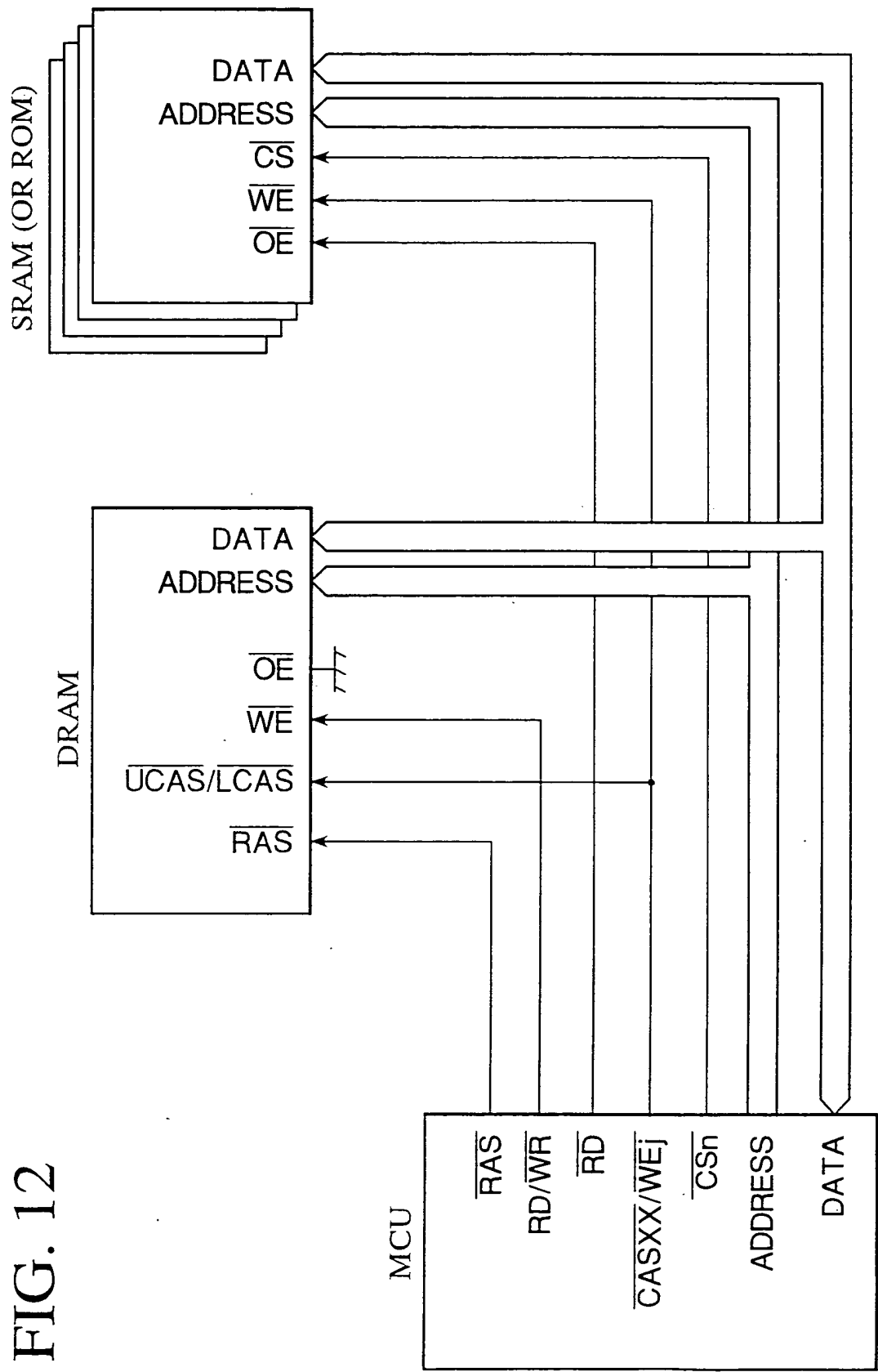


FIG. 12

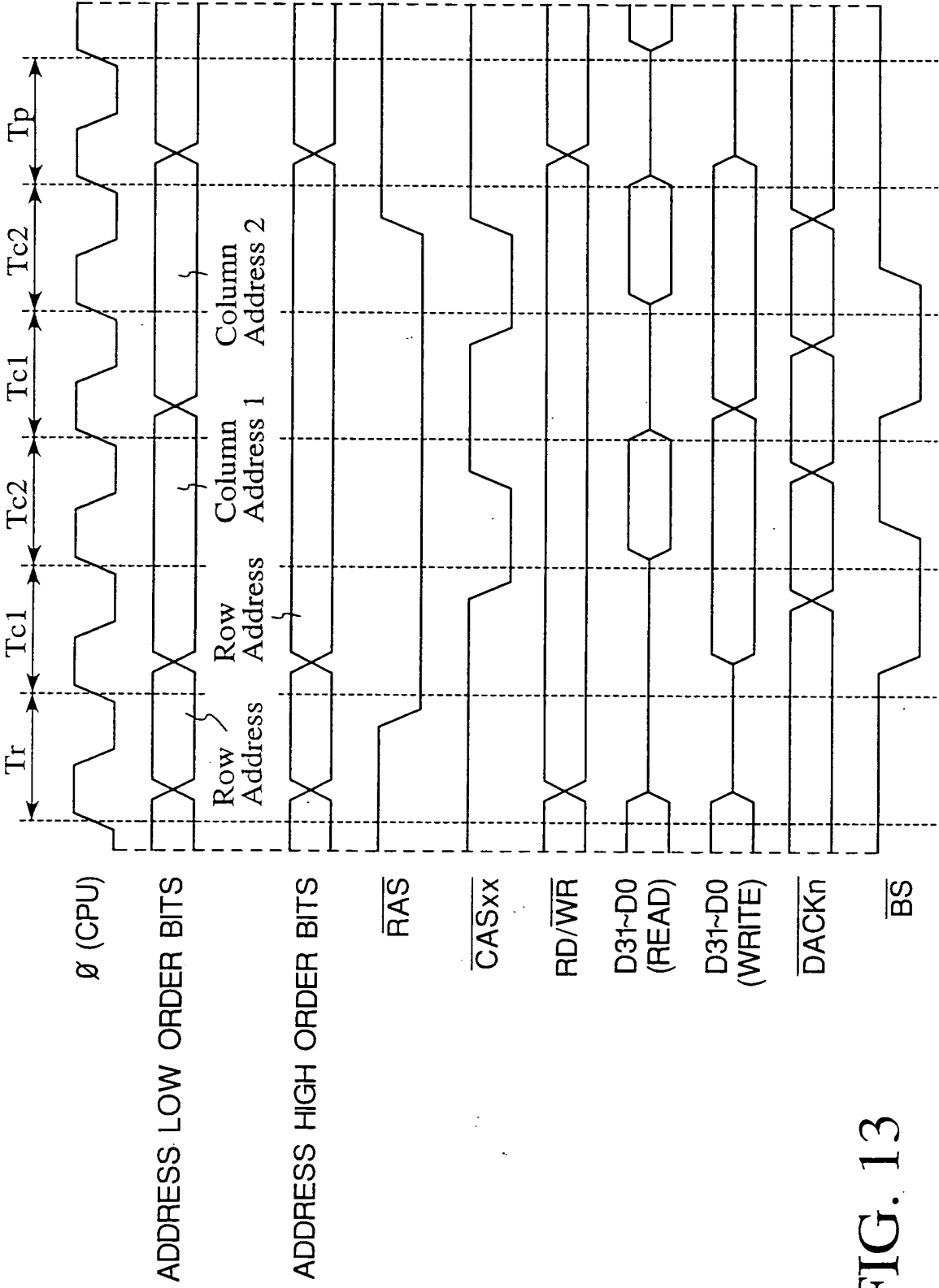


FIG. 13

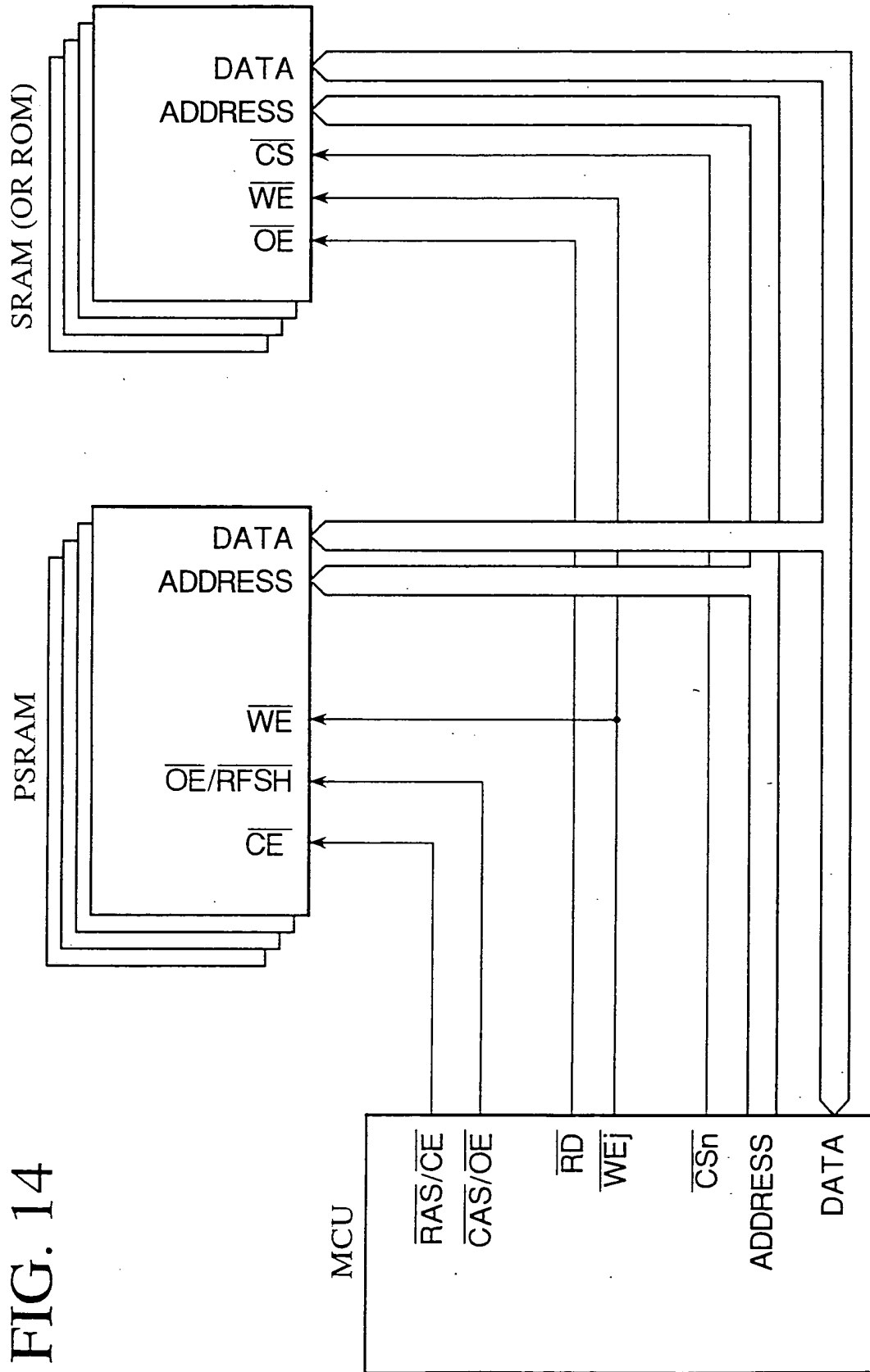


FIG. 14

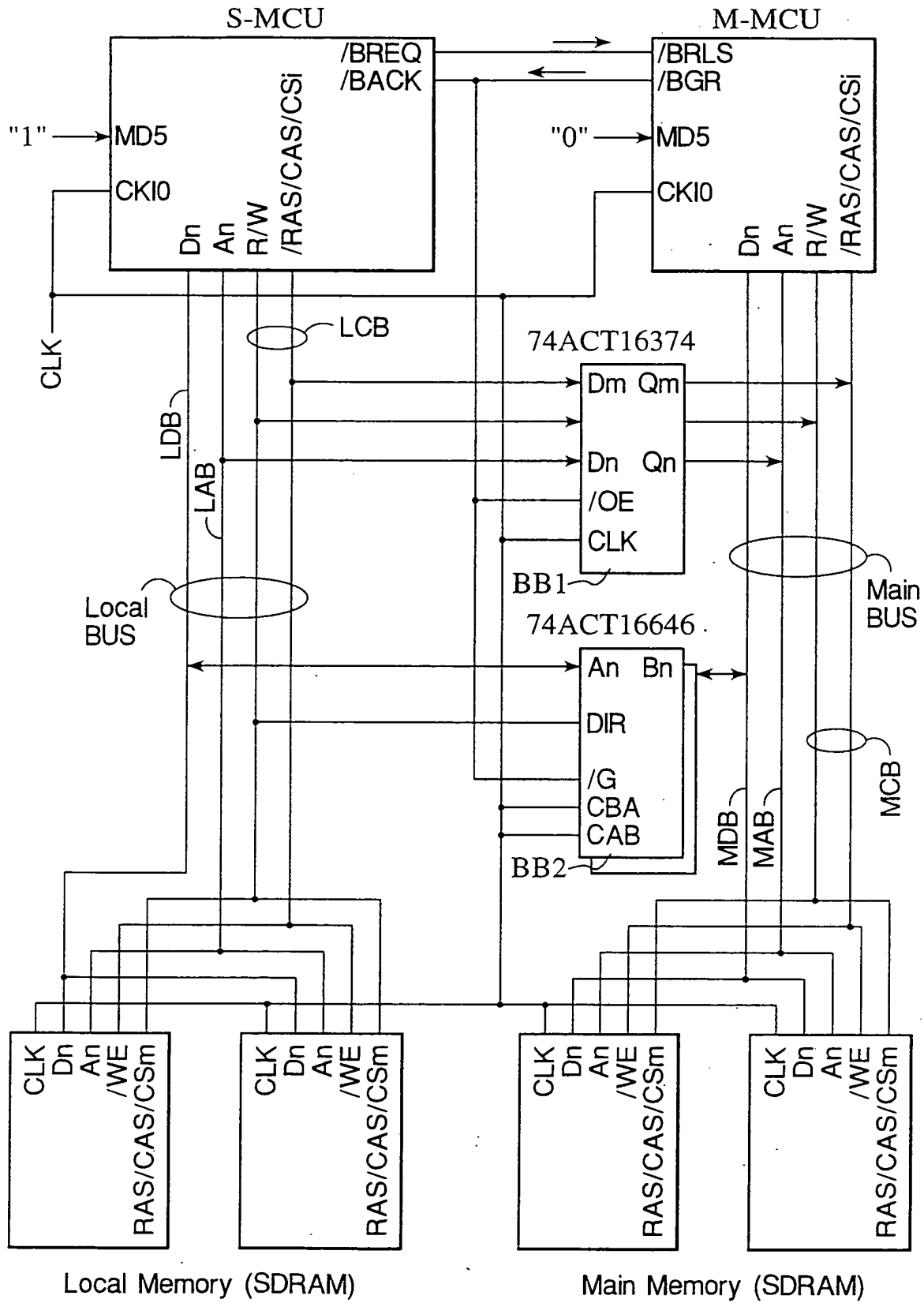


FIG. 15

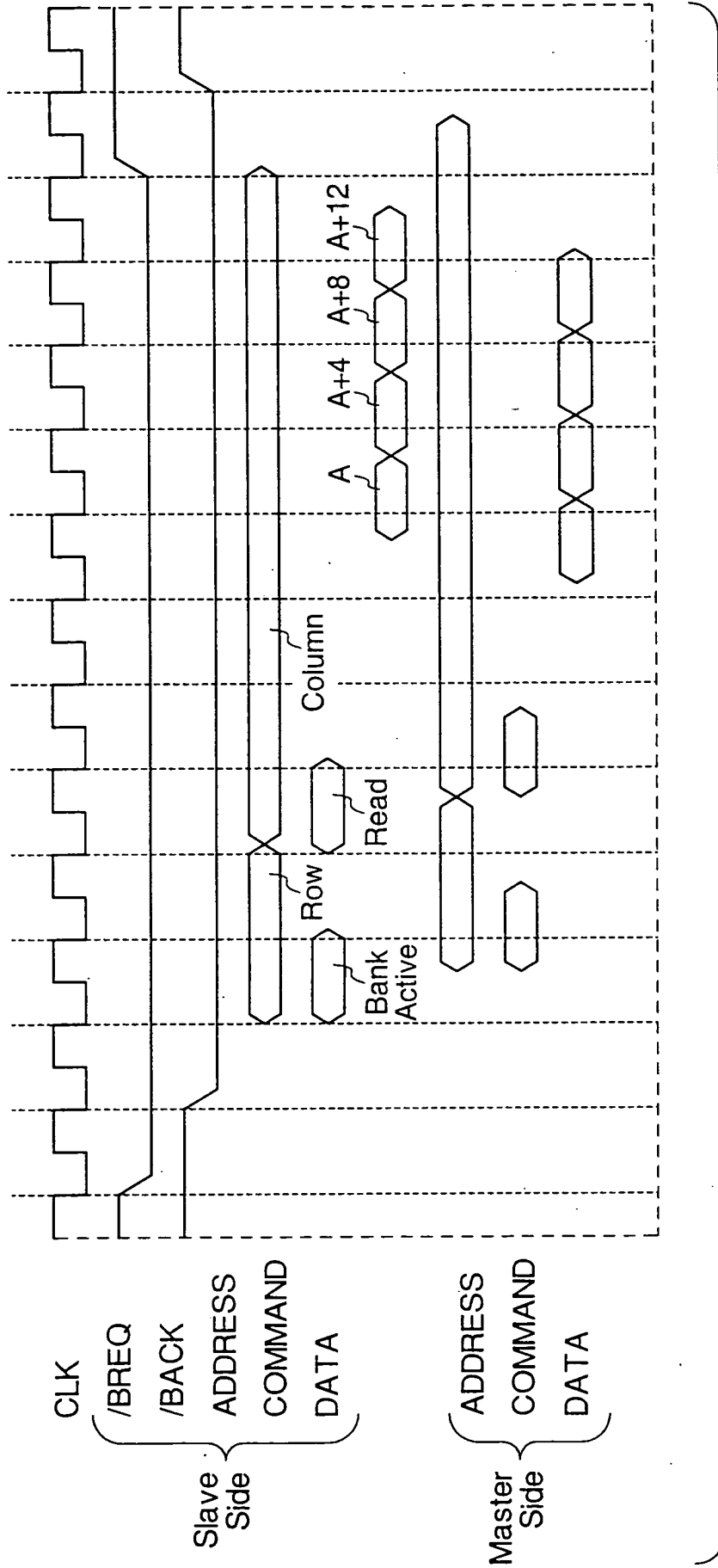


FIG. 16



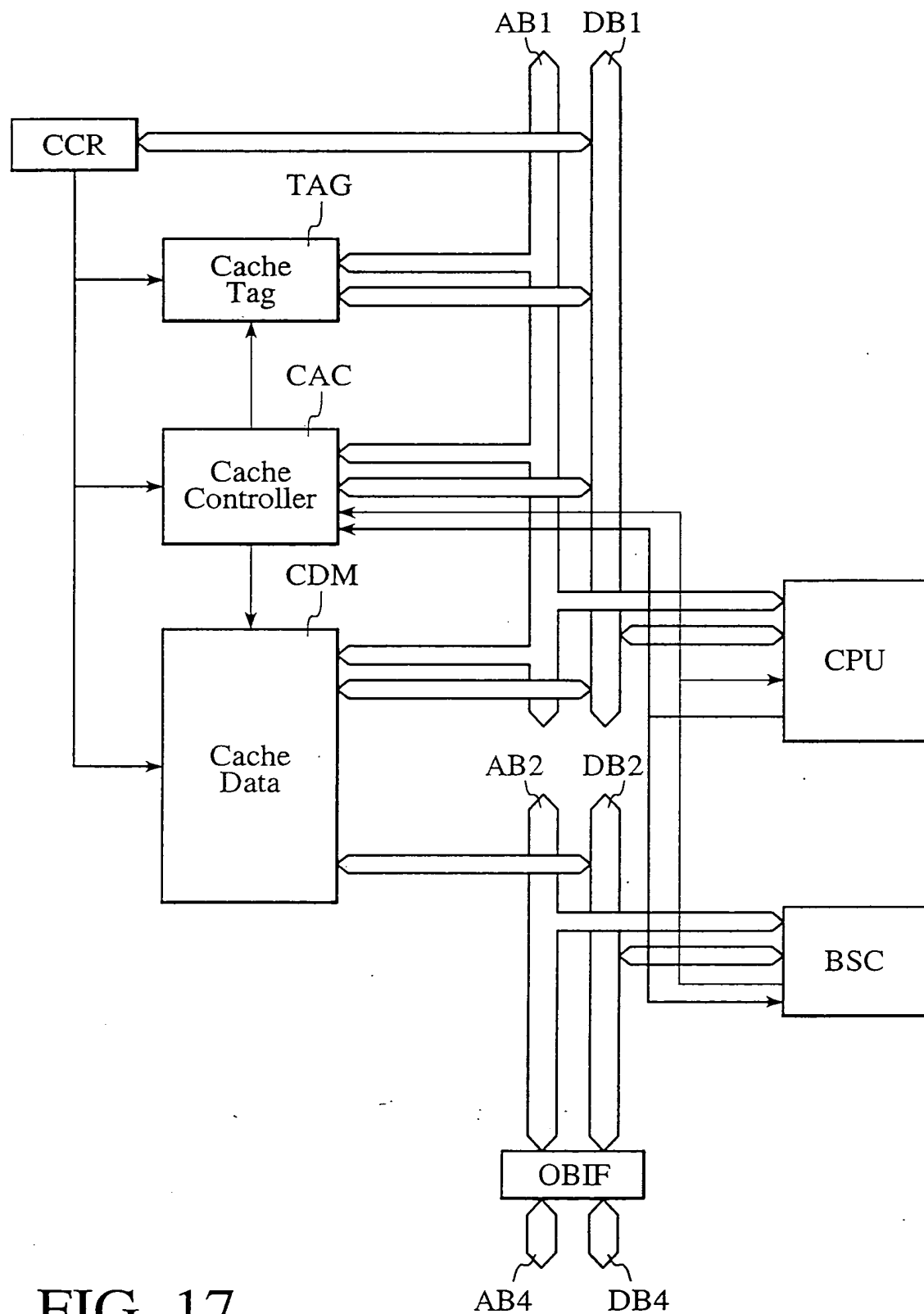


FIG. 17

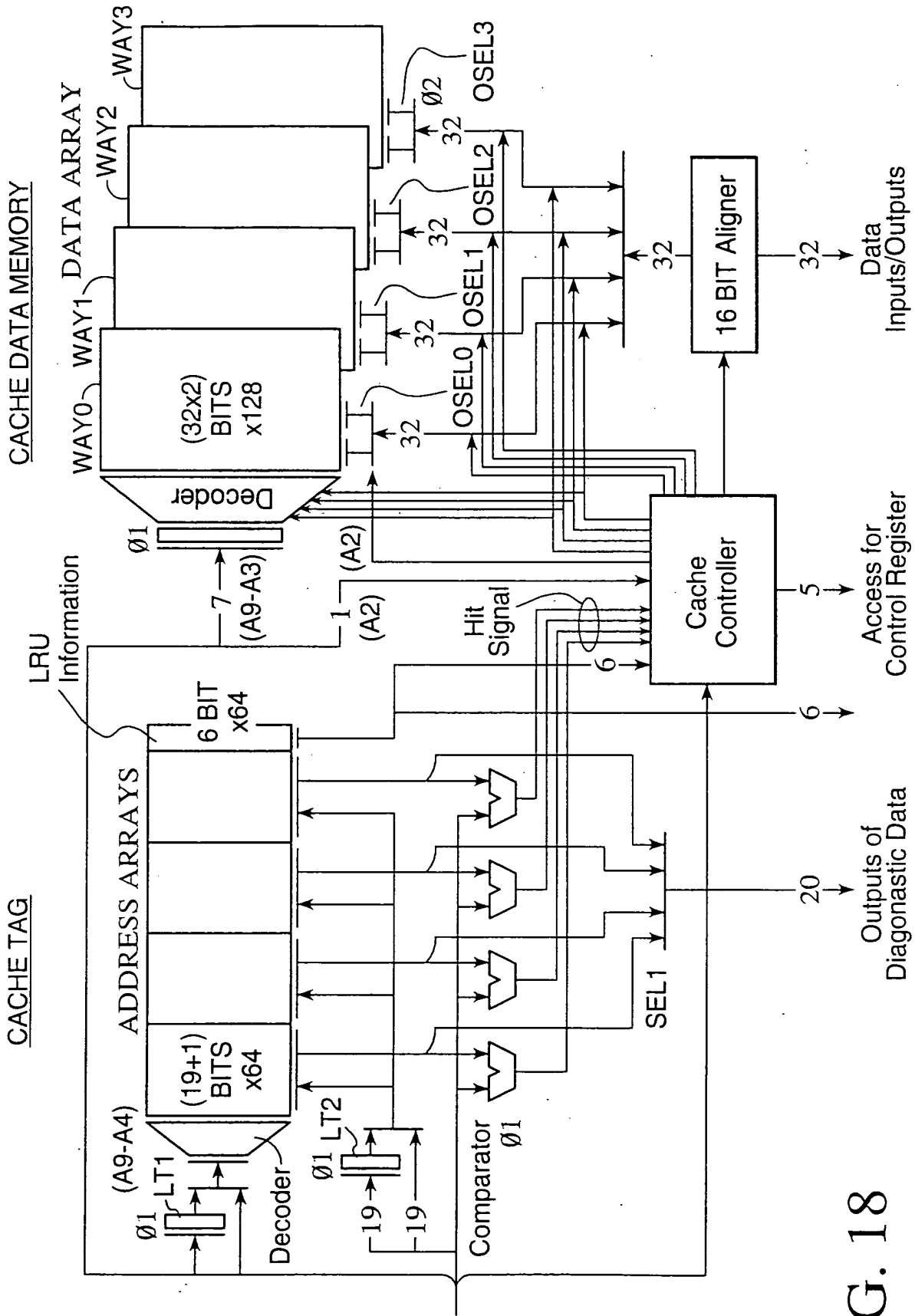


FIG. 18



FIG. 19

FIG. 20

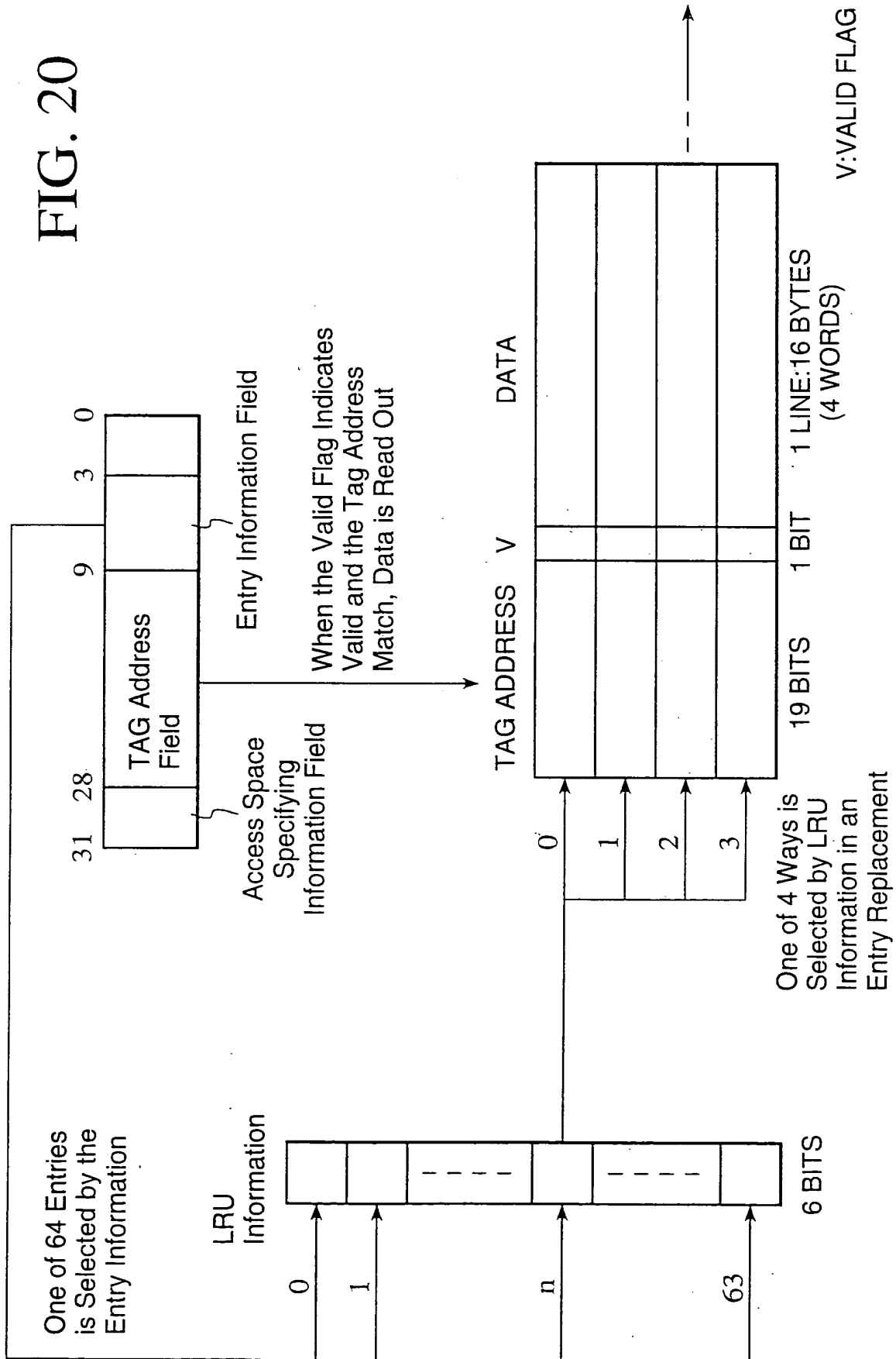
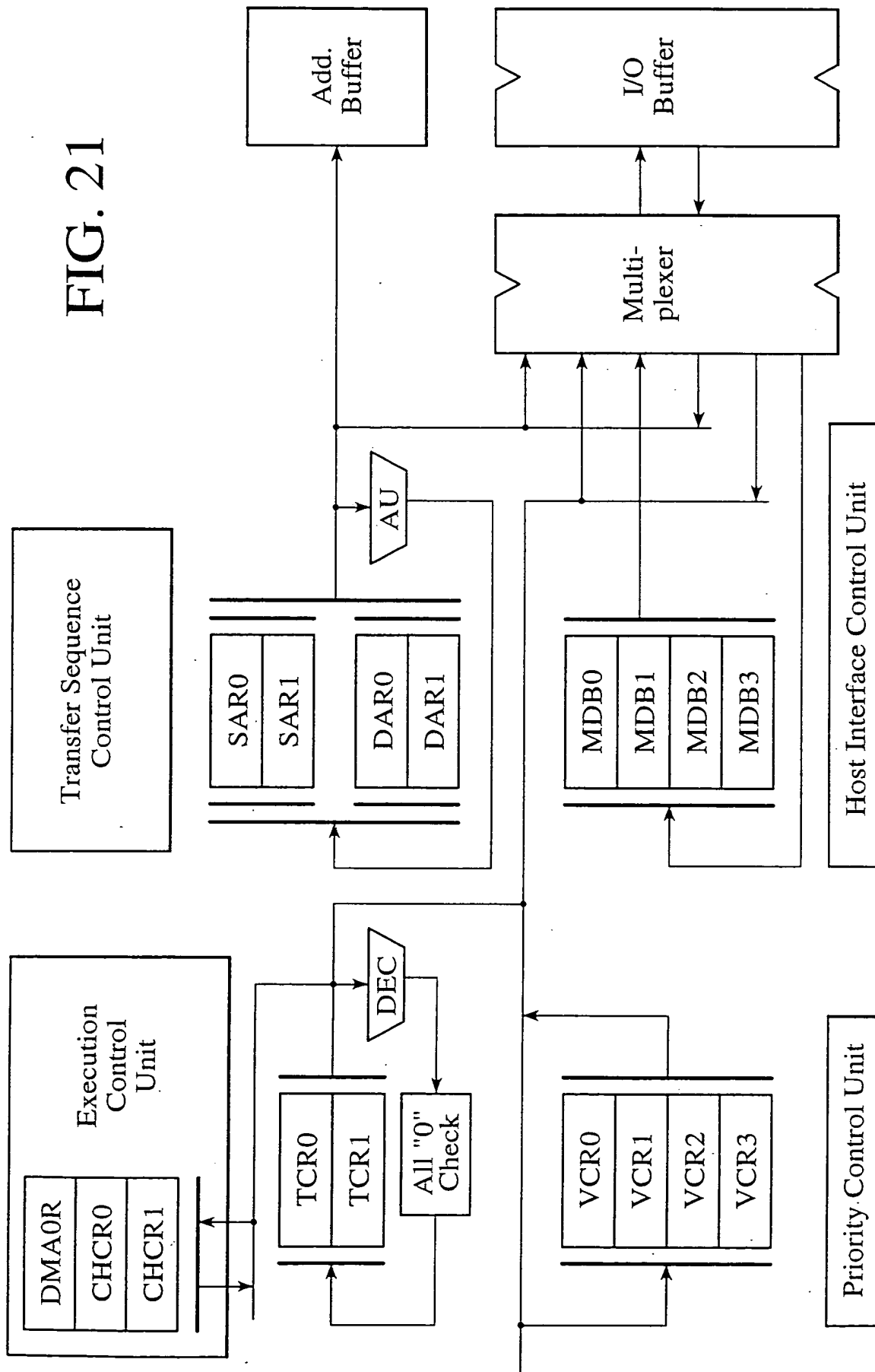


FIG. 21



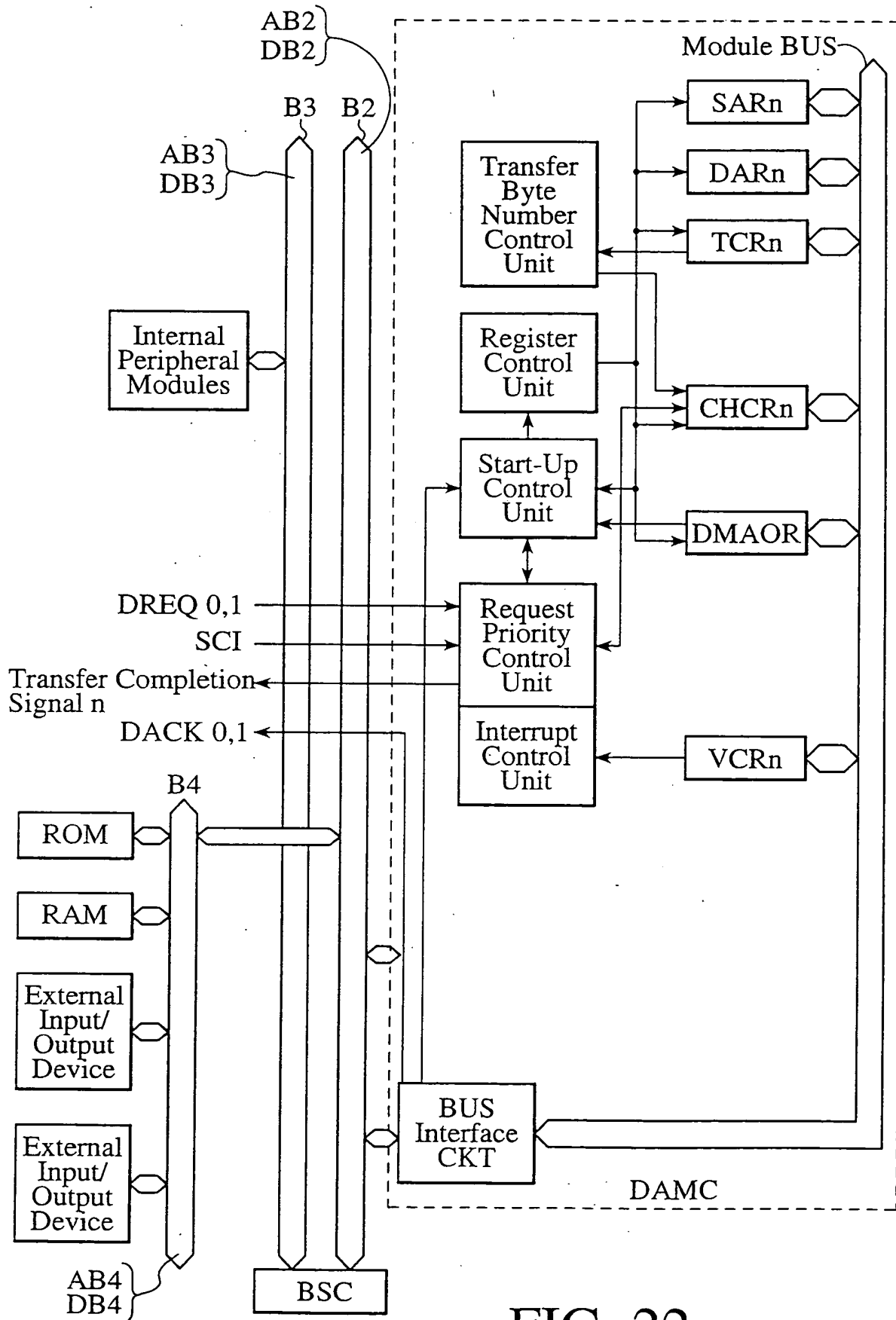


FIG. 22

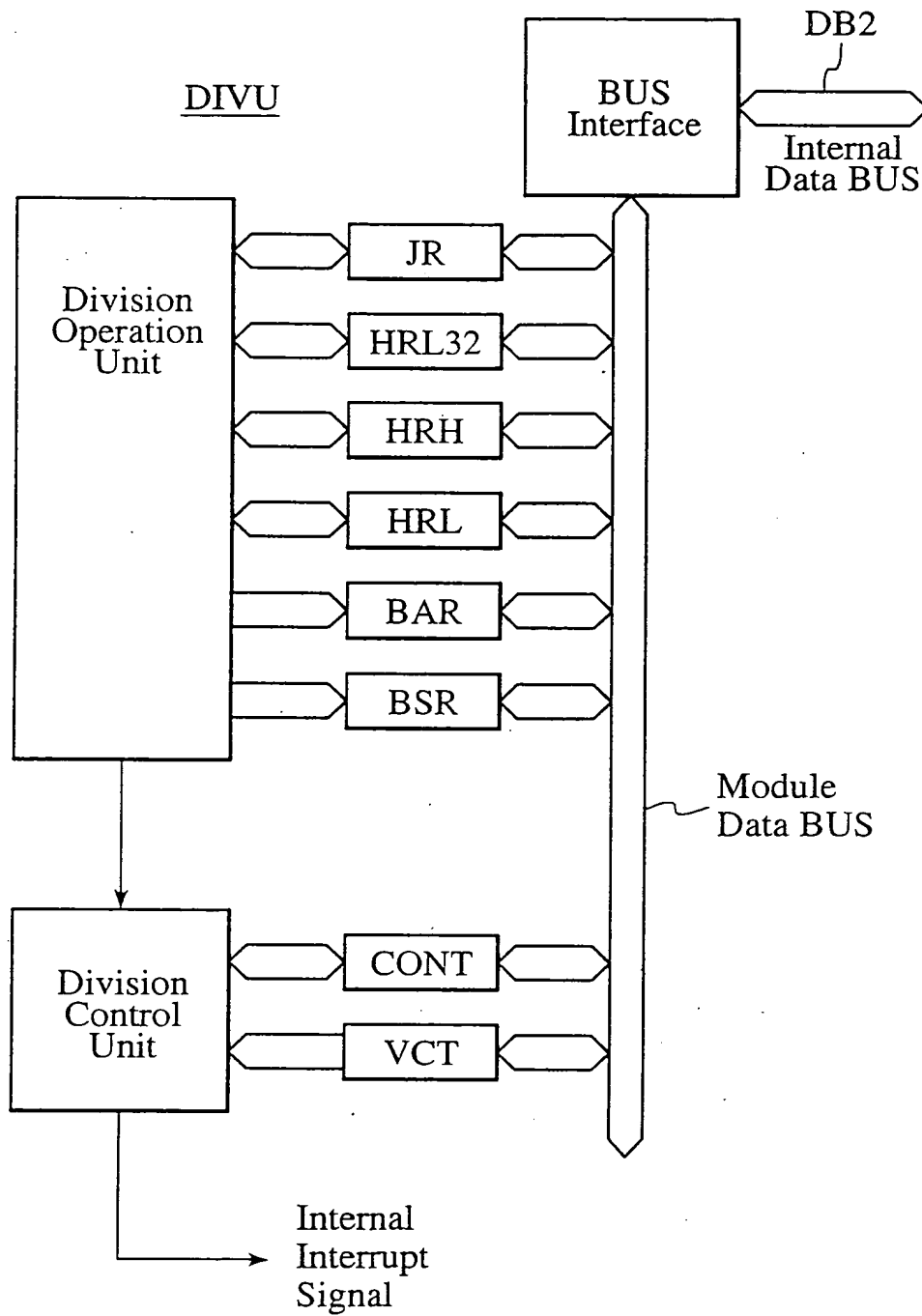
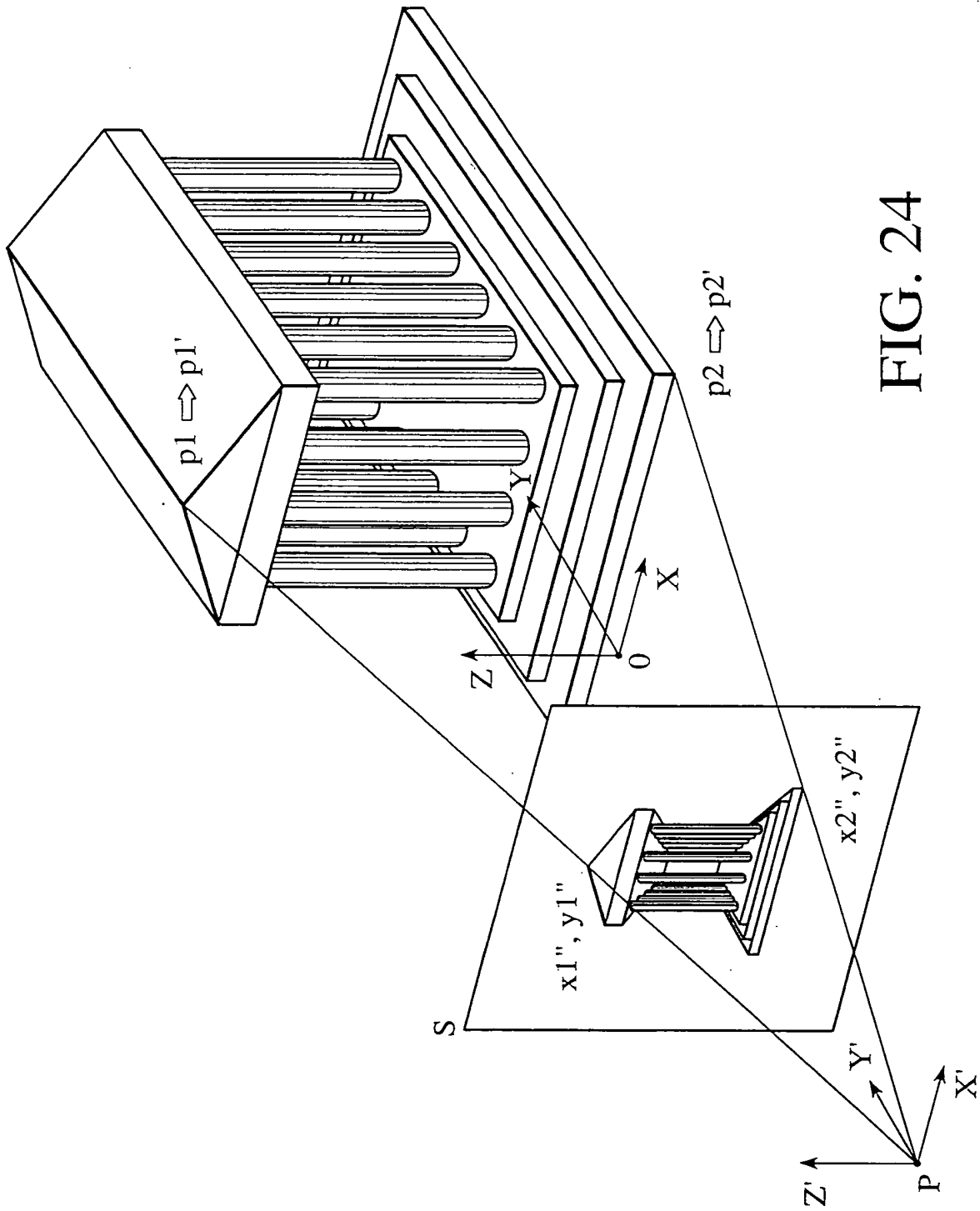


FIG. 23





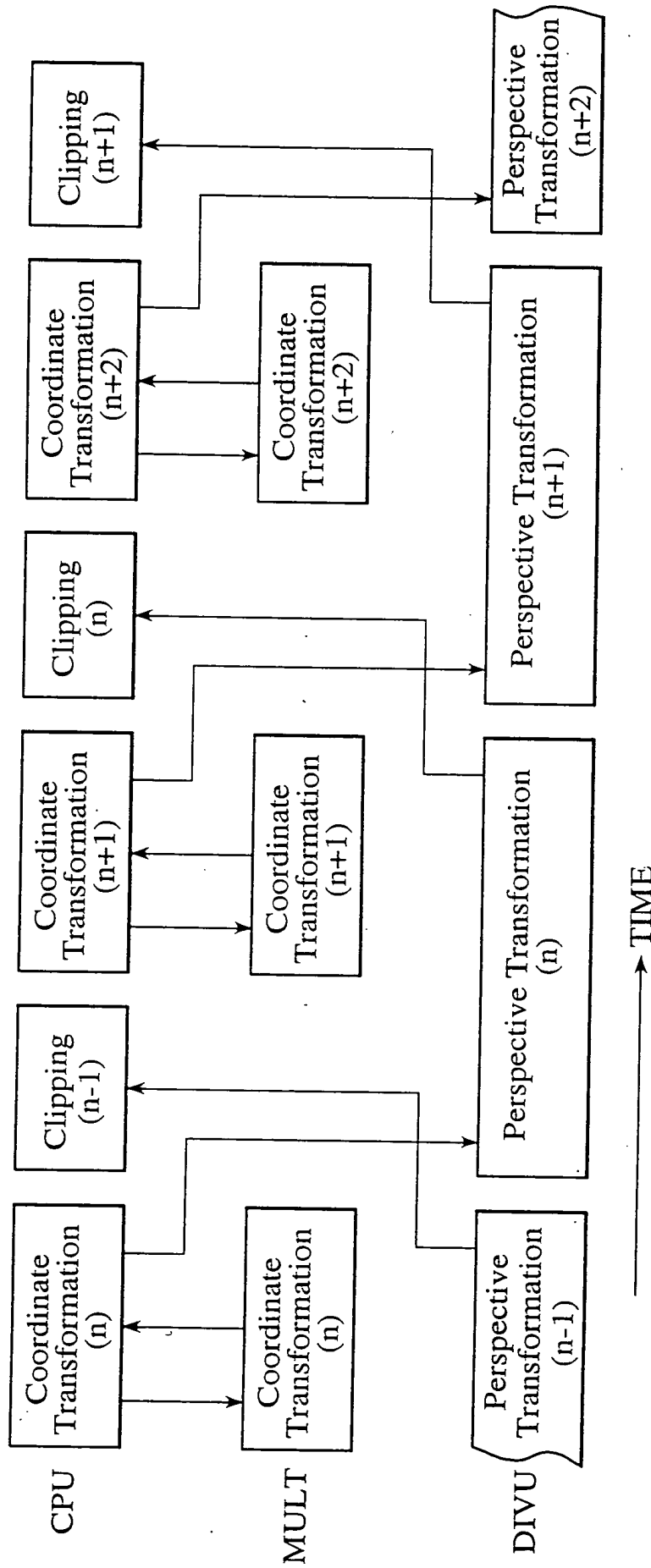


FIG. 25

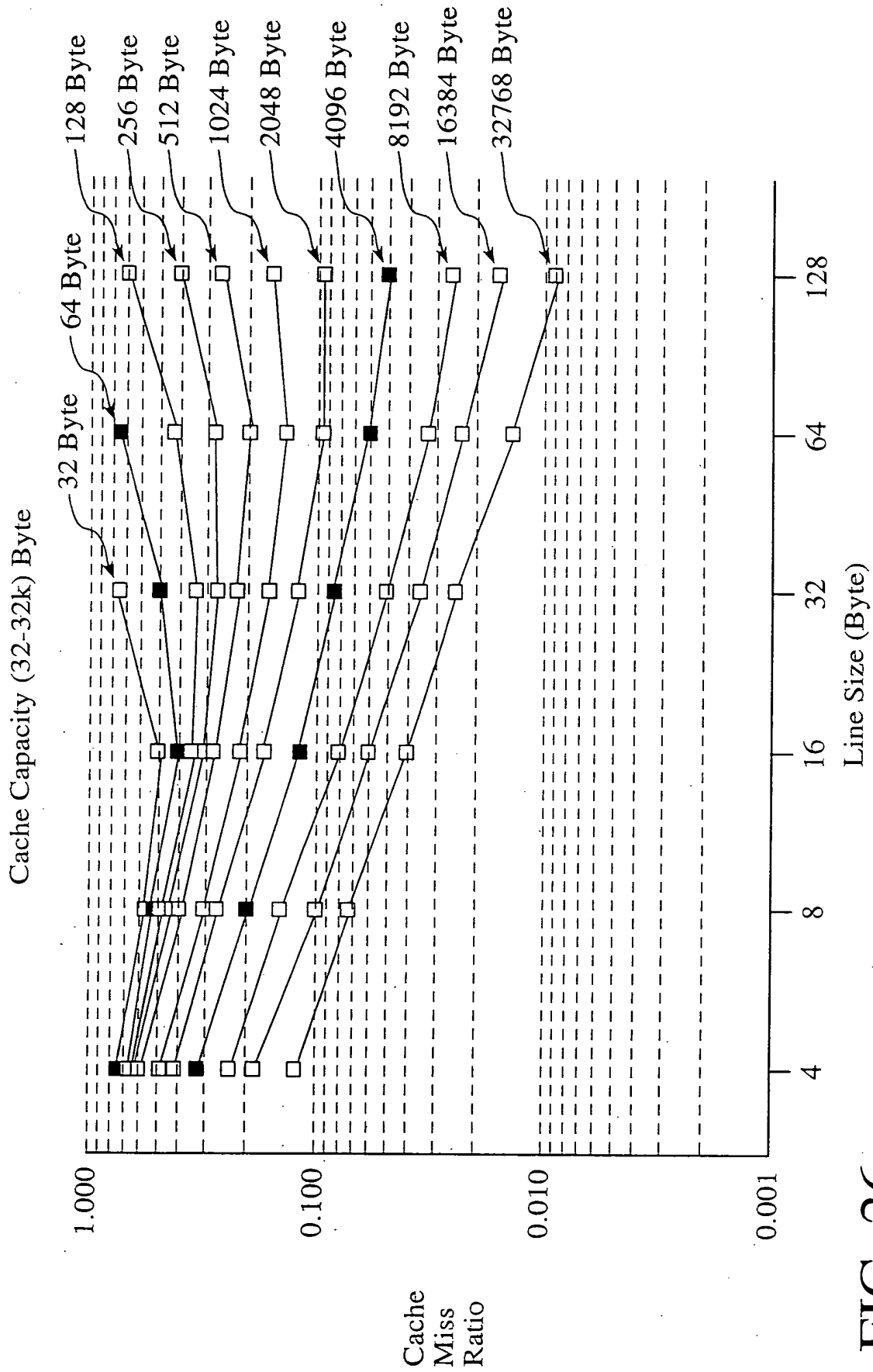


FIG. 26

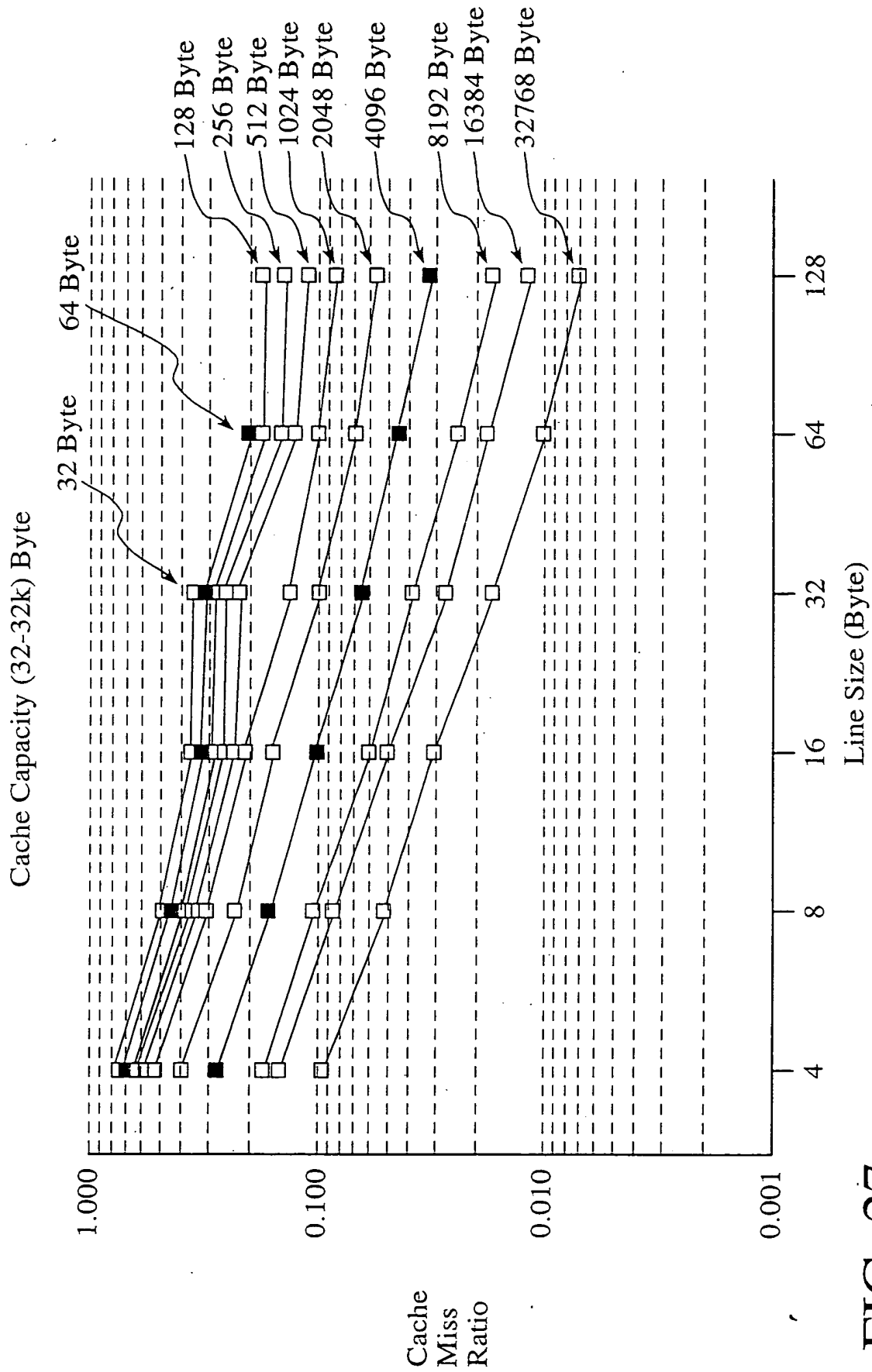


FIG. 27

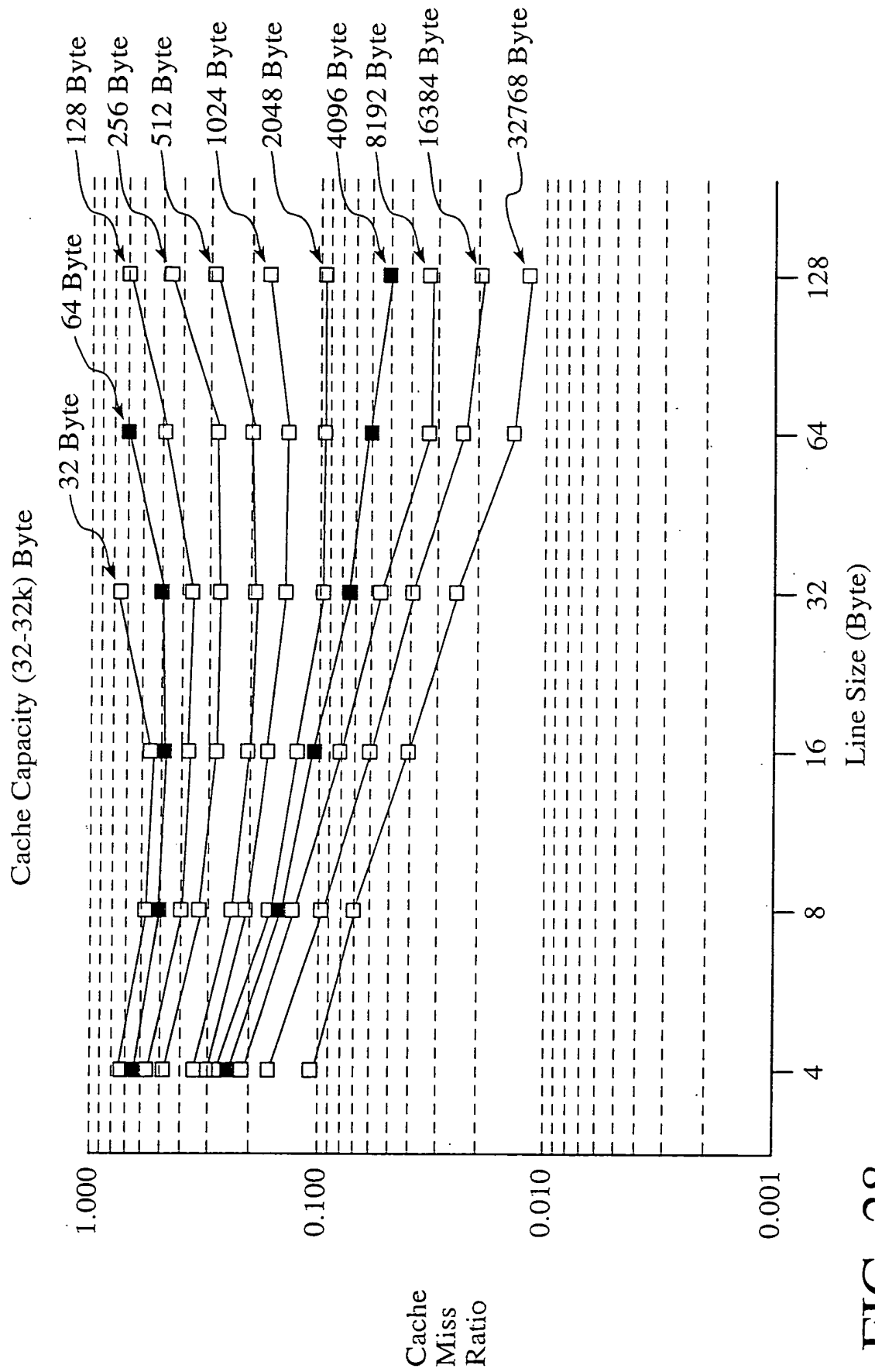


FIG. 28



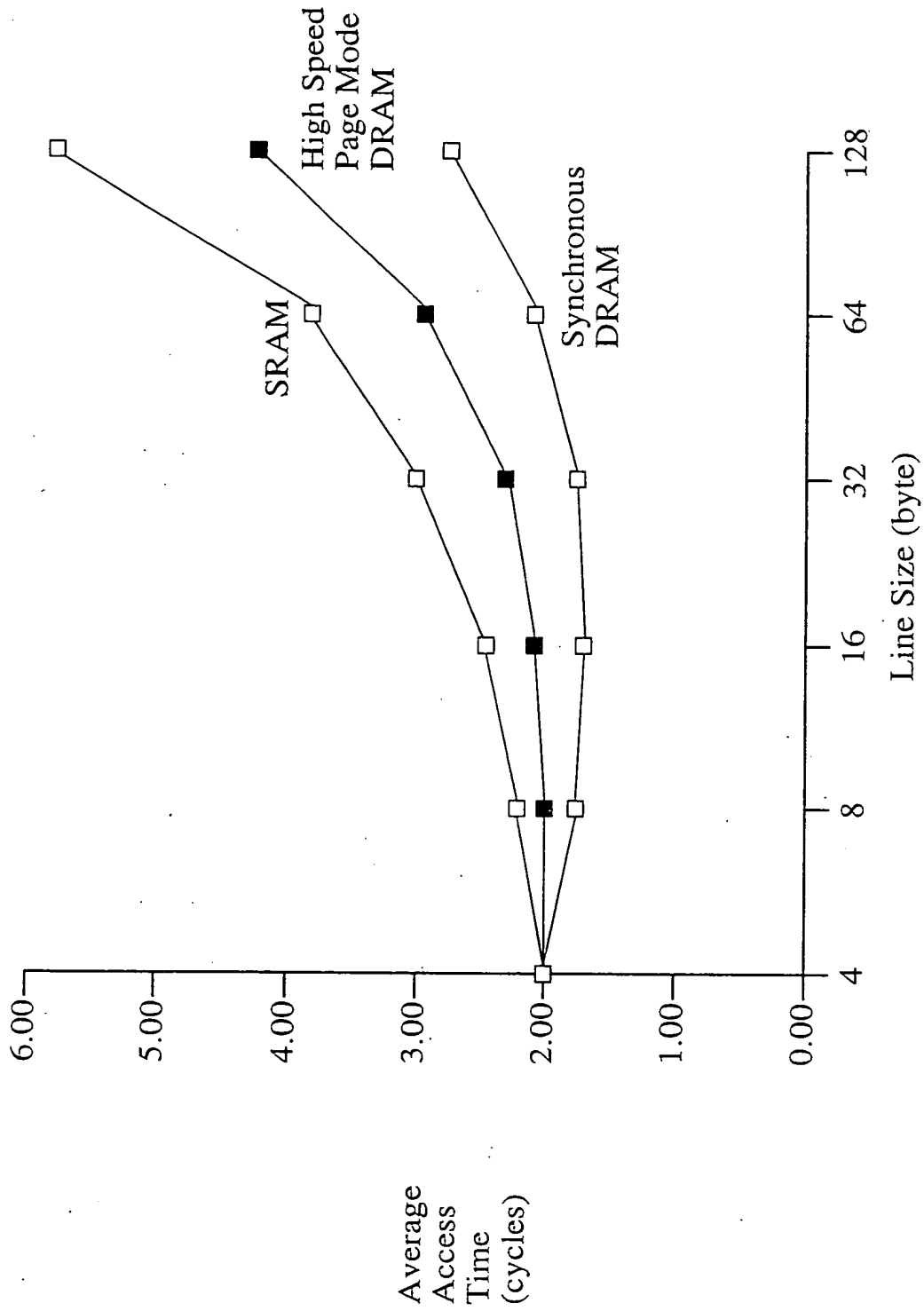


FIG. 30

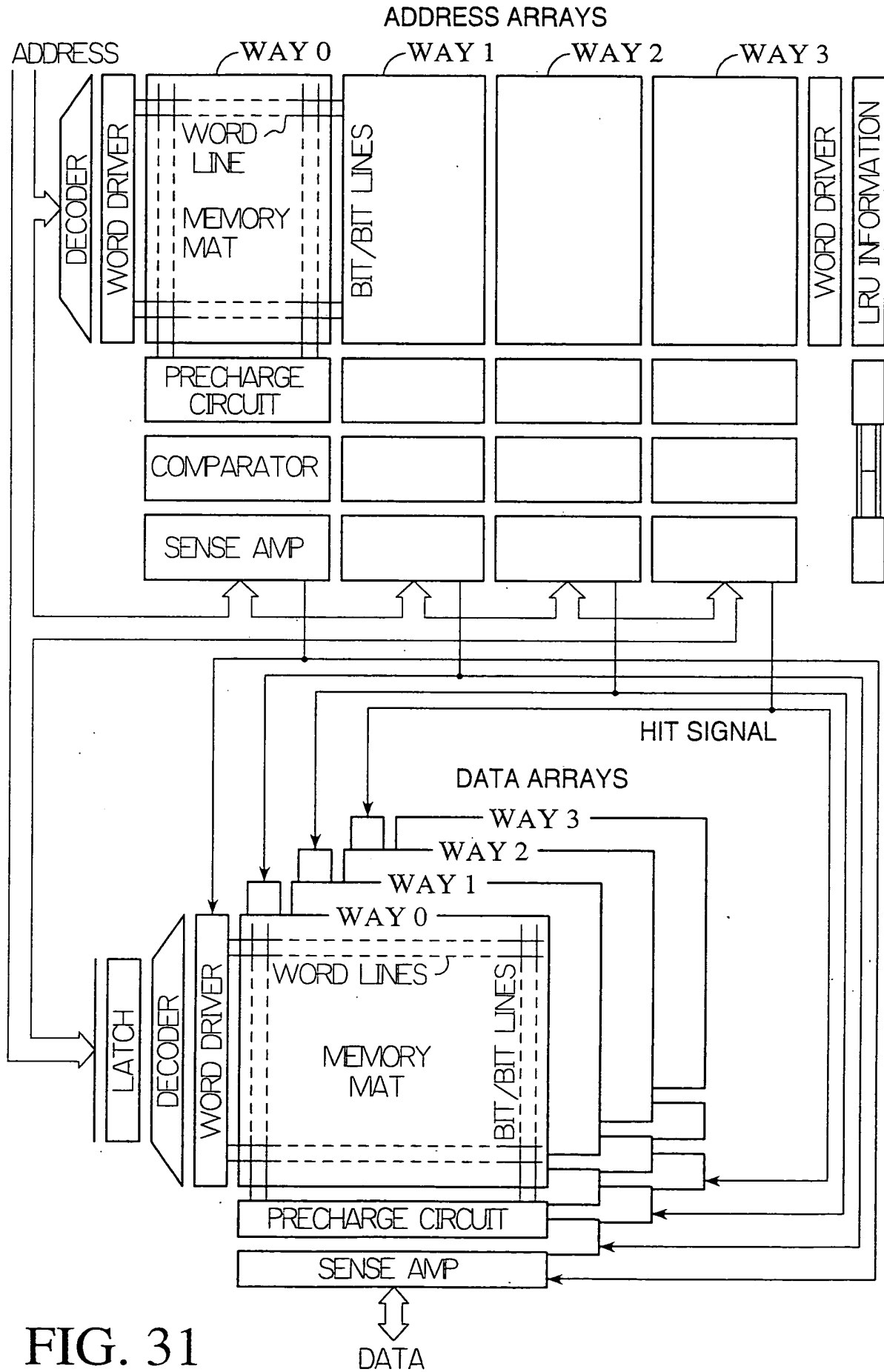
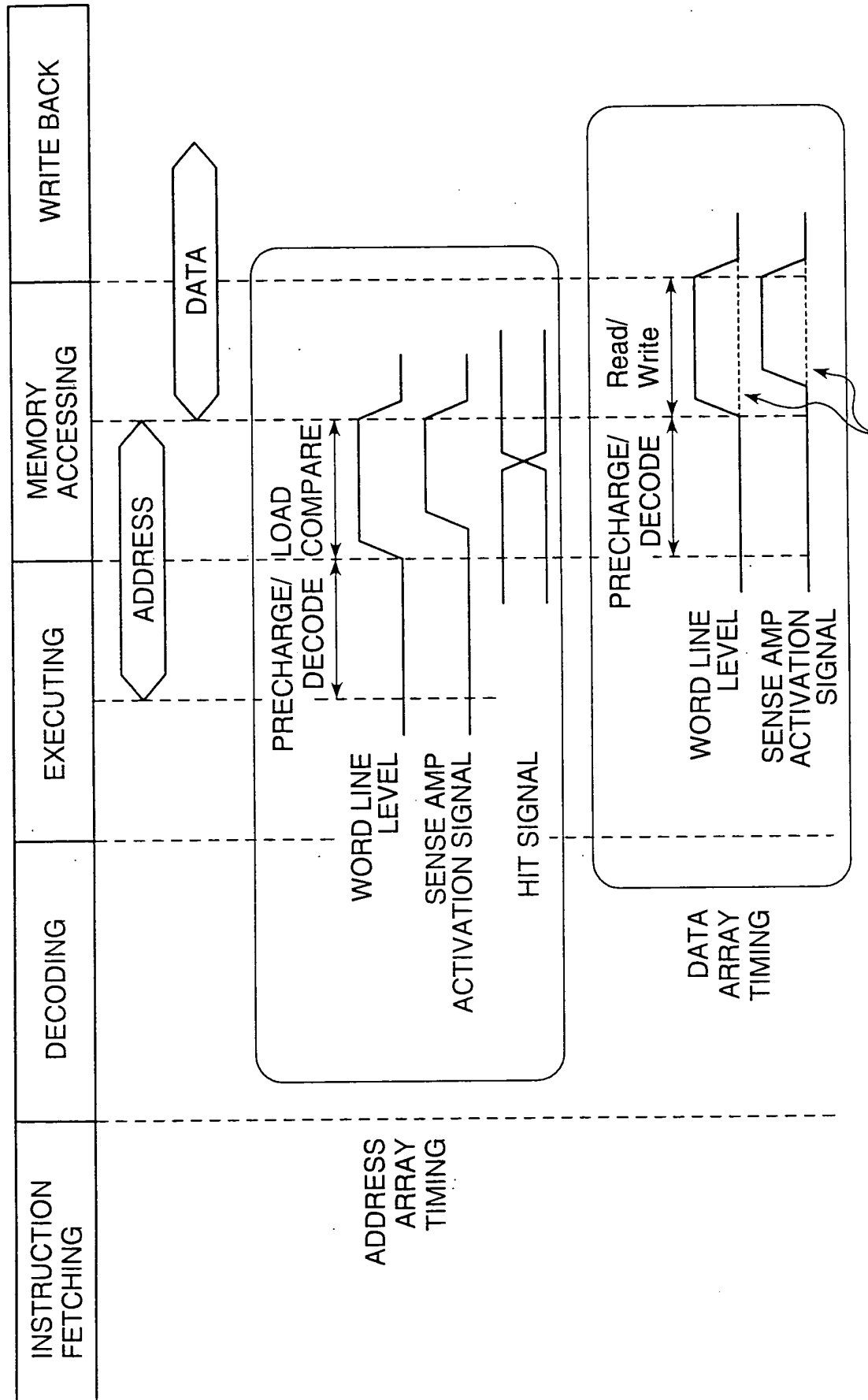


FIG. 31



DOTTED LINES INDICATE THE WORD LINE LEVEL AND THE SENSE AMP ACTIVATION SIGNAL ON NO HIT WAYS

FIG. 32



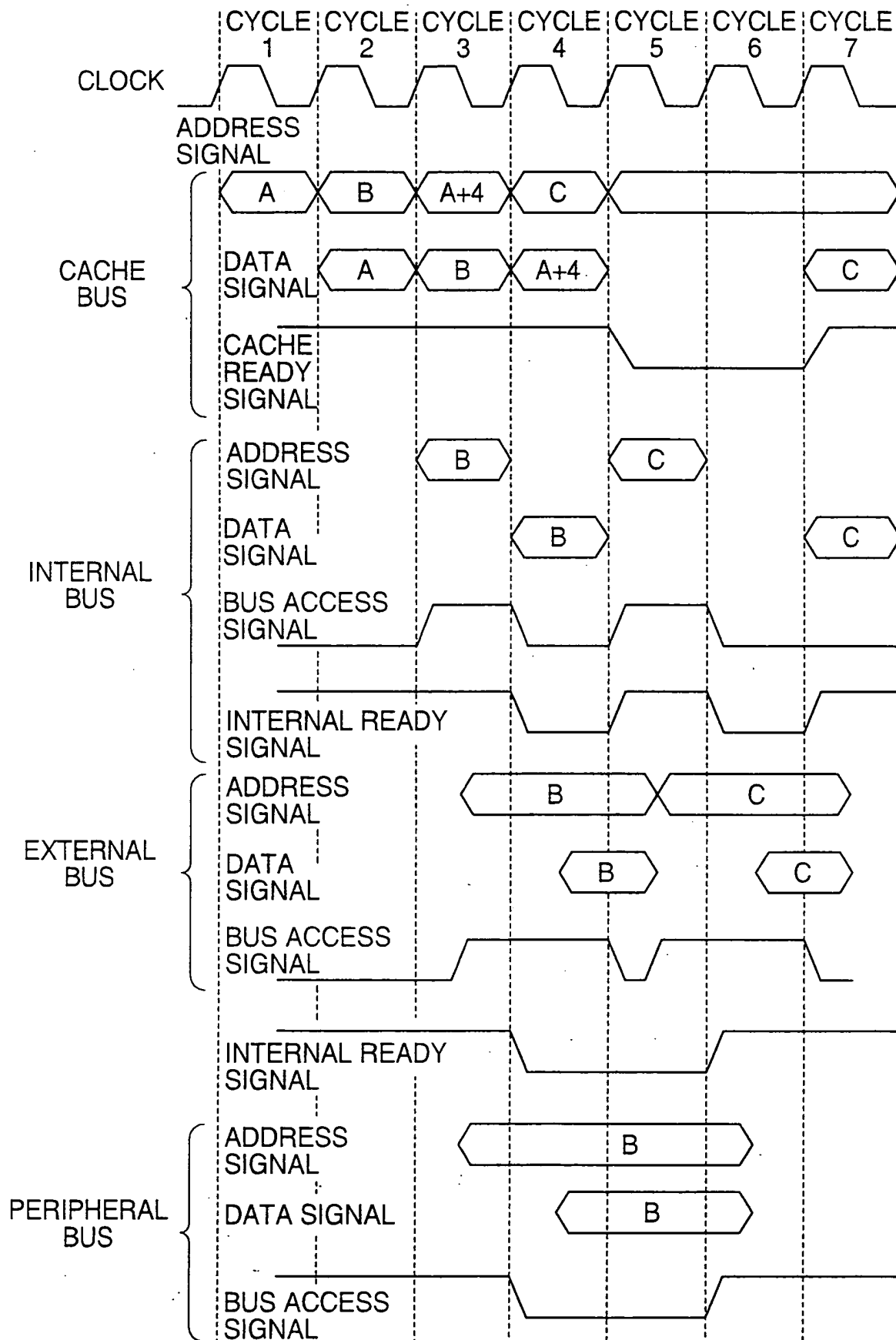


FIG. 33

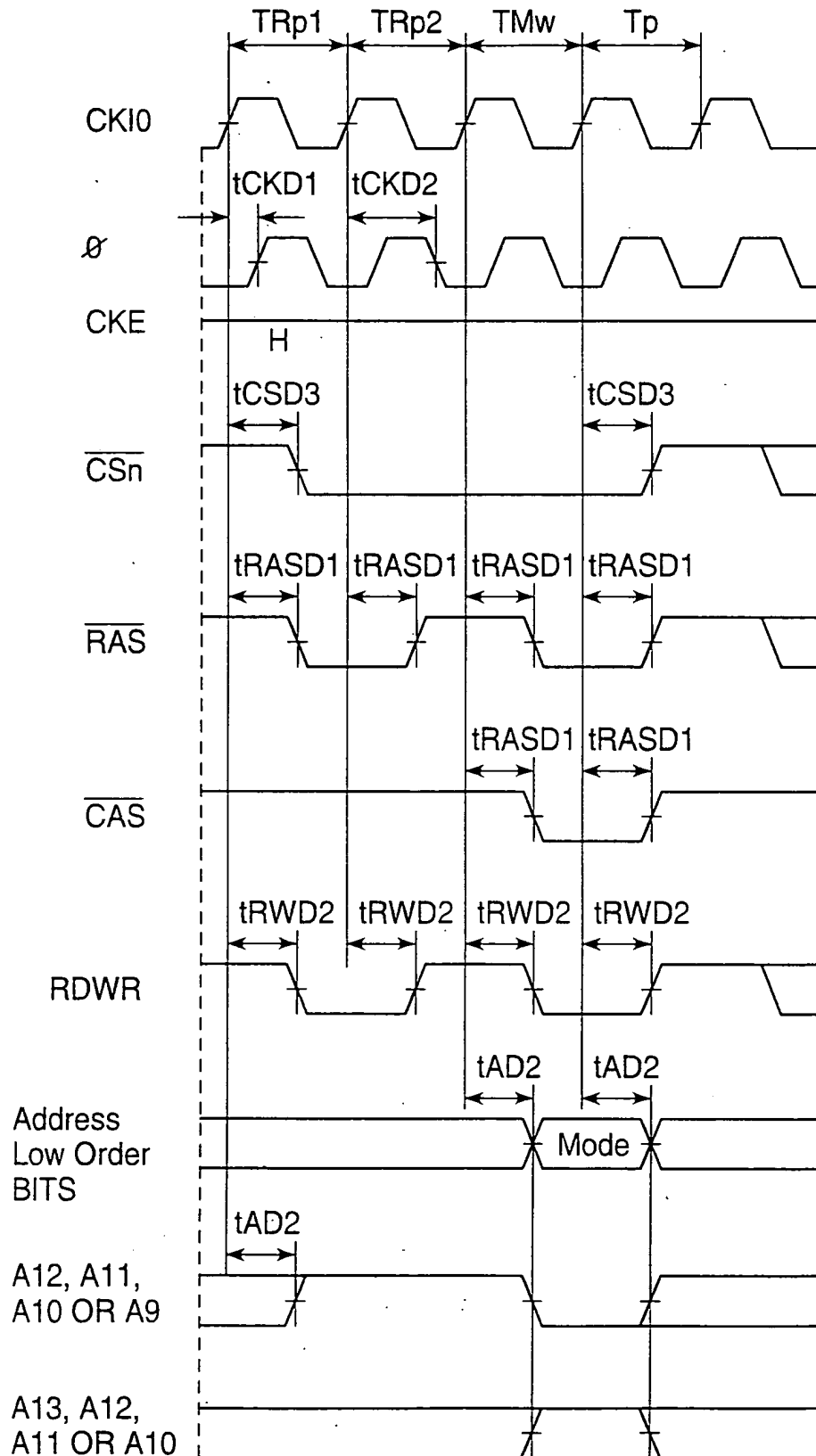
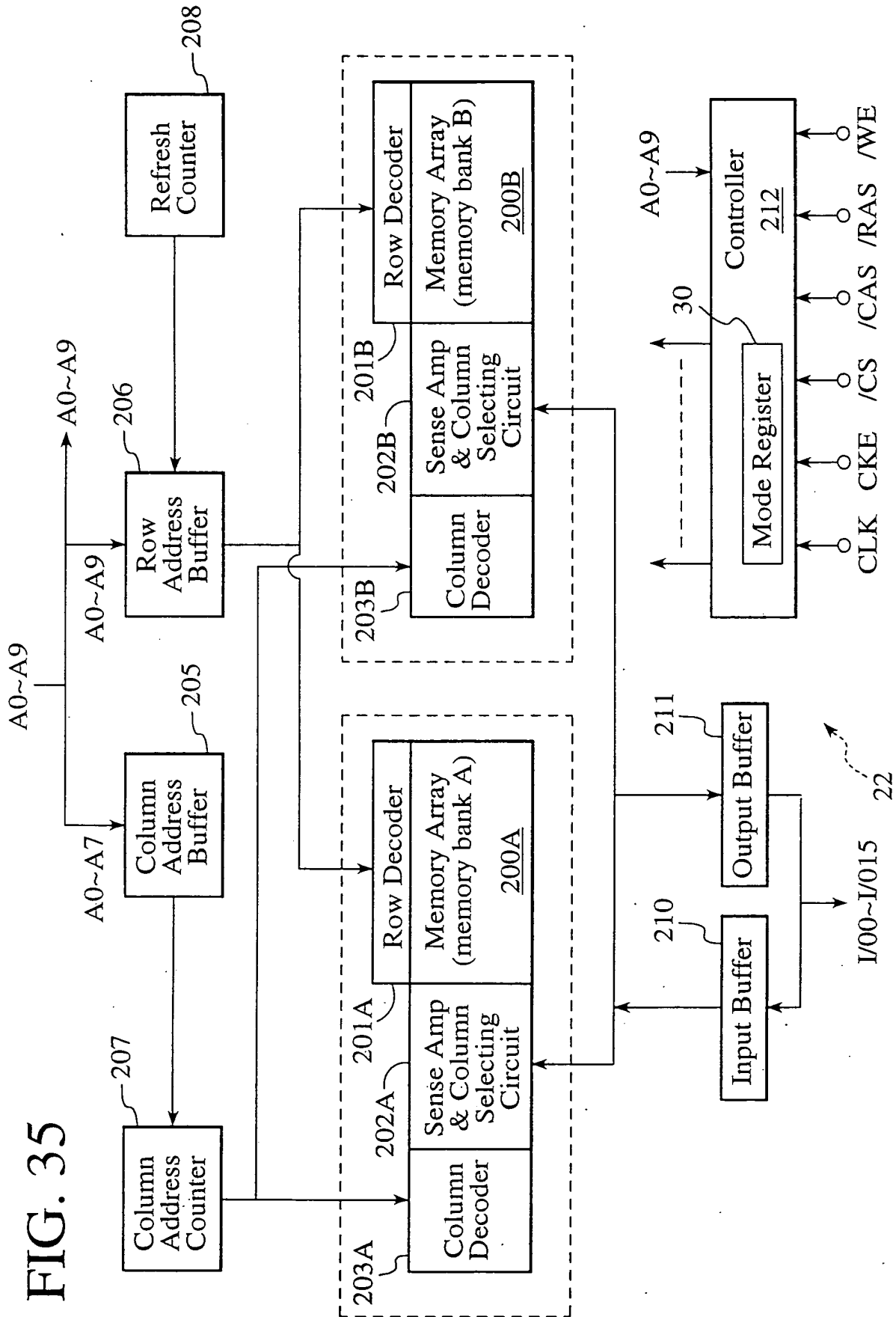


FIG. 34

FIG. 35



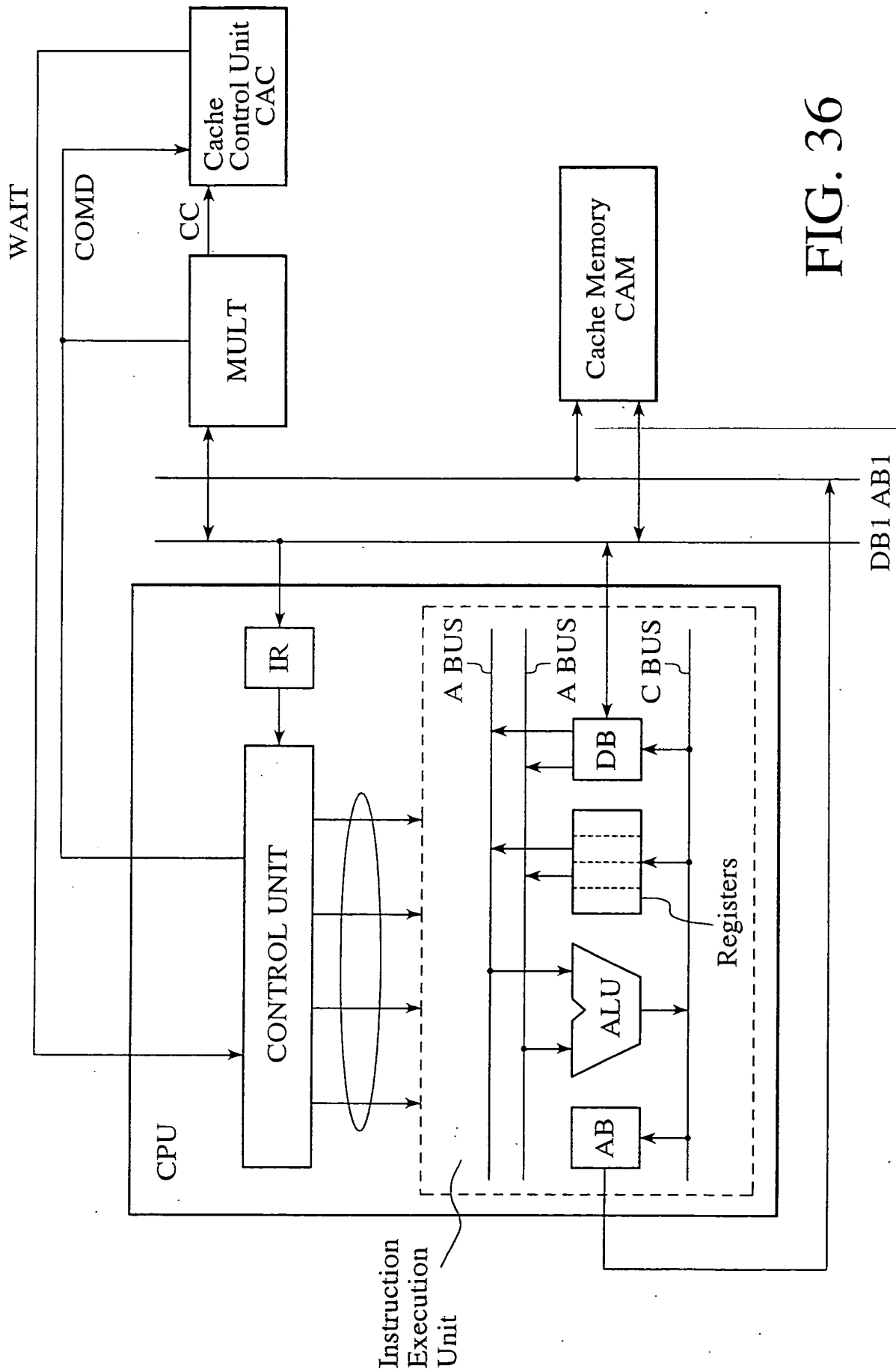


FIG. 36

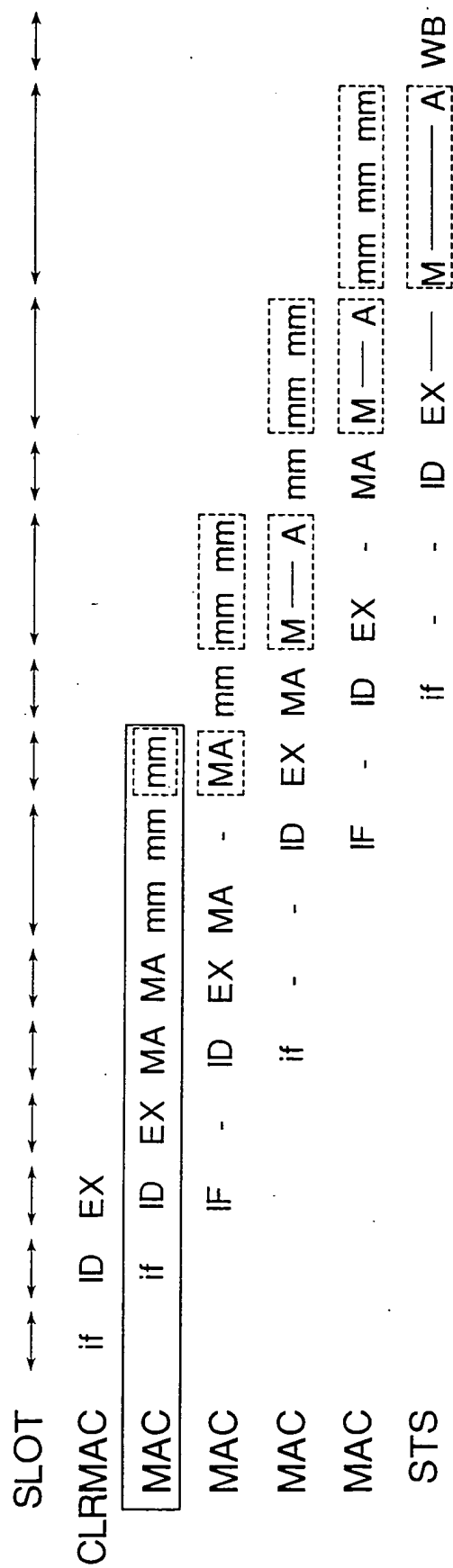


FIG. 37

FIG. 38

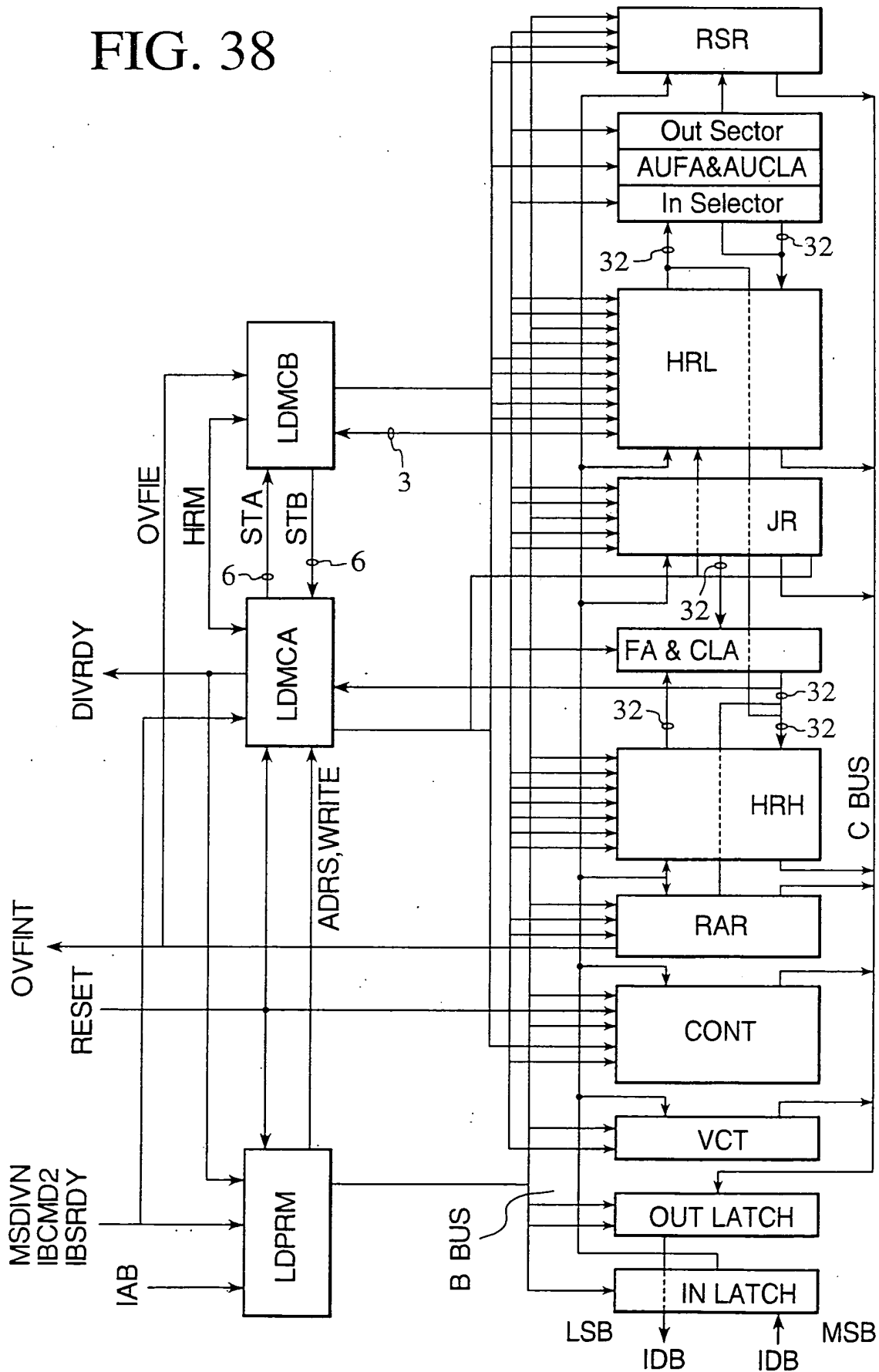


FIG. 39

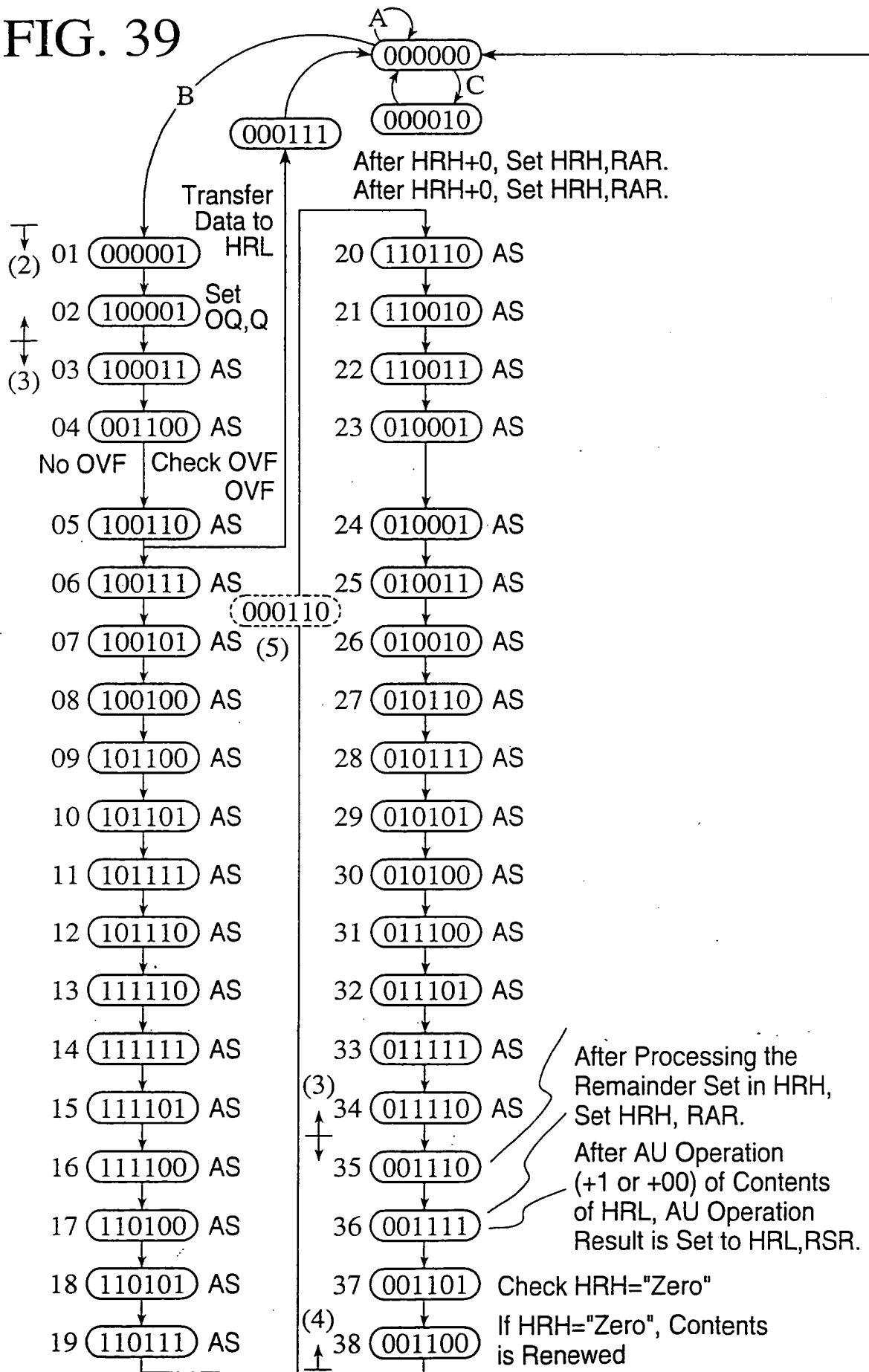
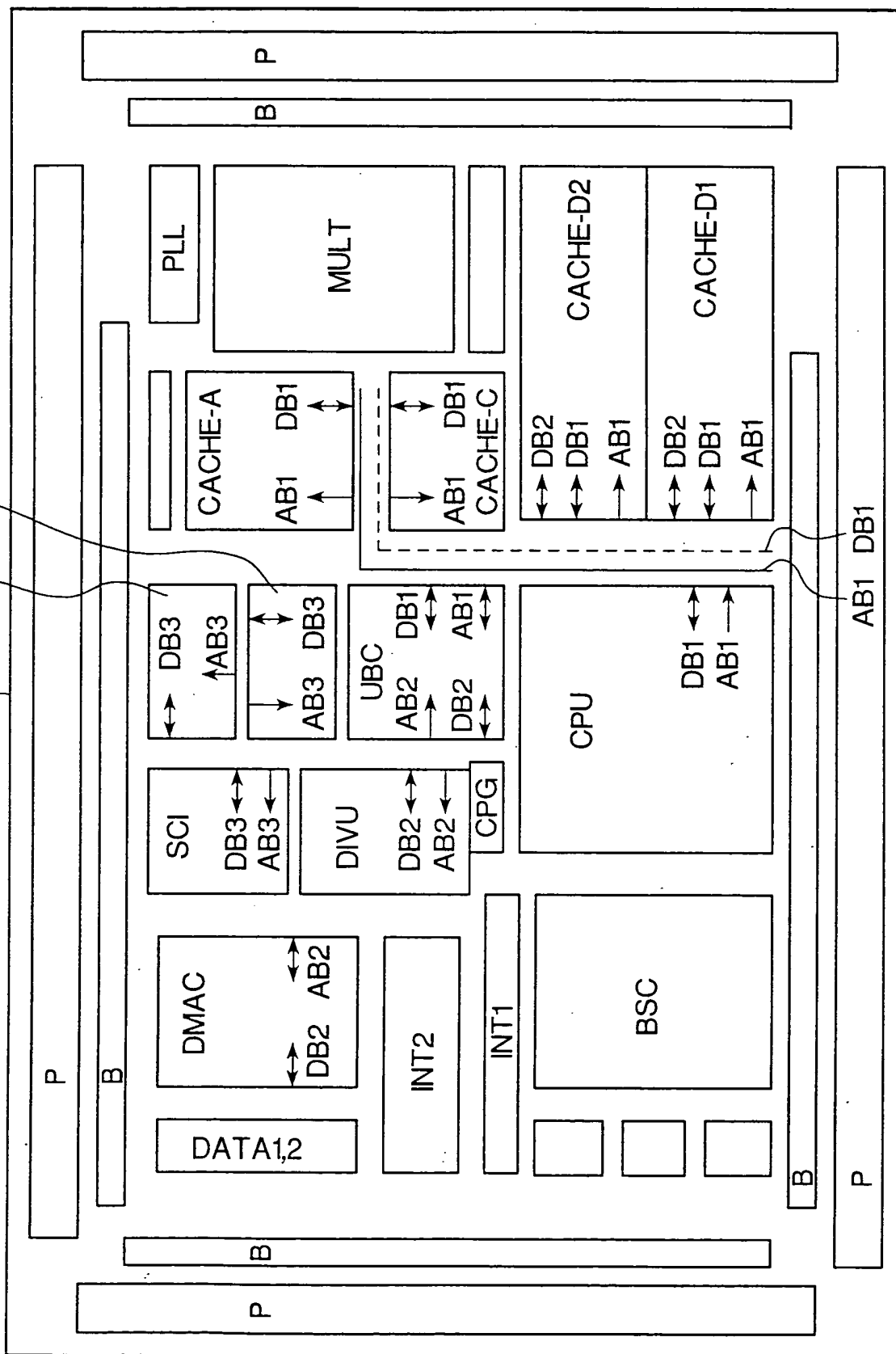


FIG. 40 Semiconductor Chip





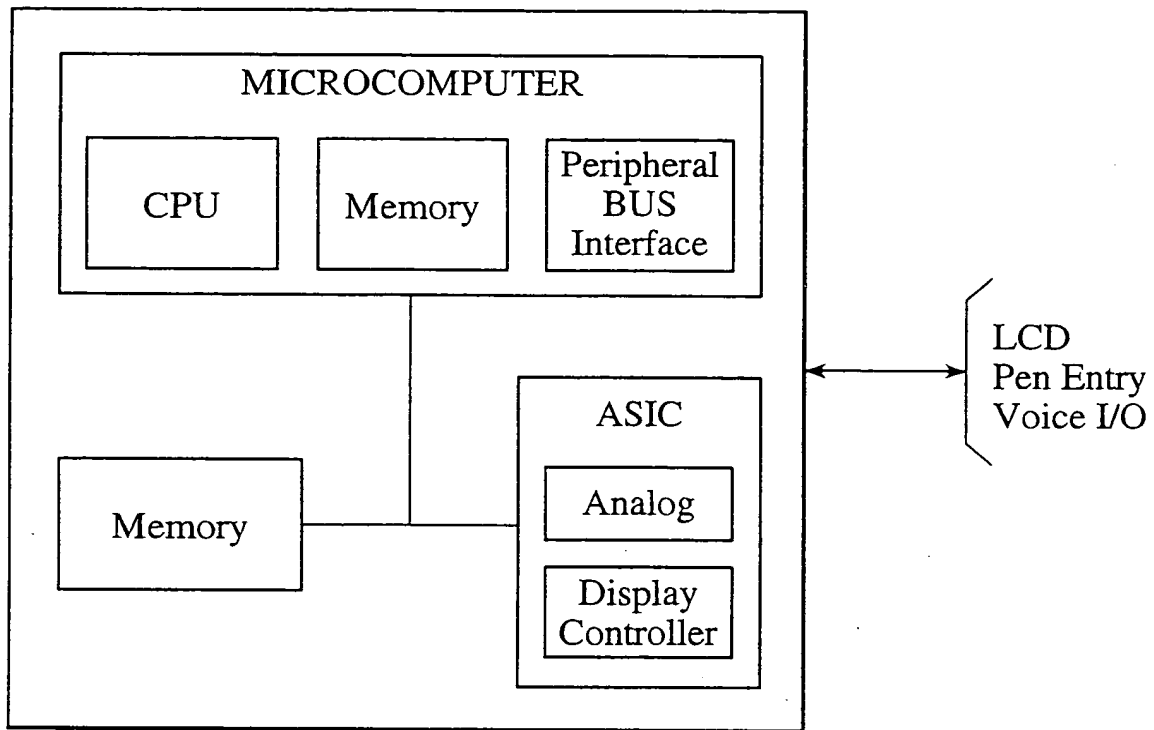


FIG. 41A

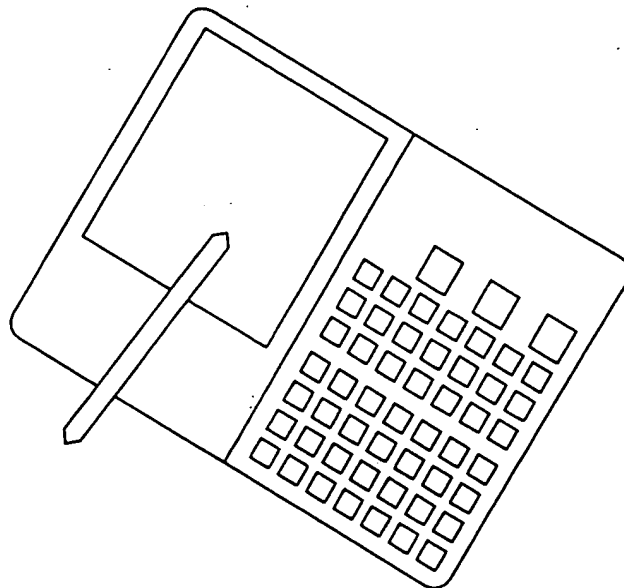


FIG. 41B

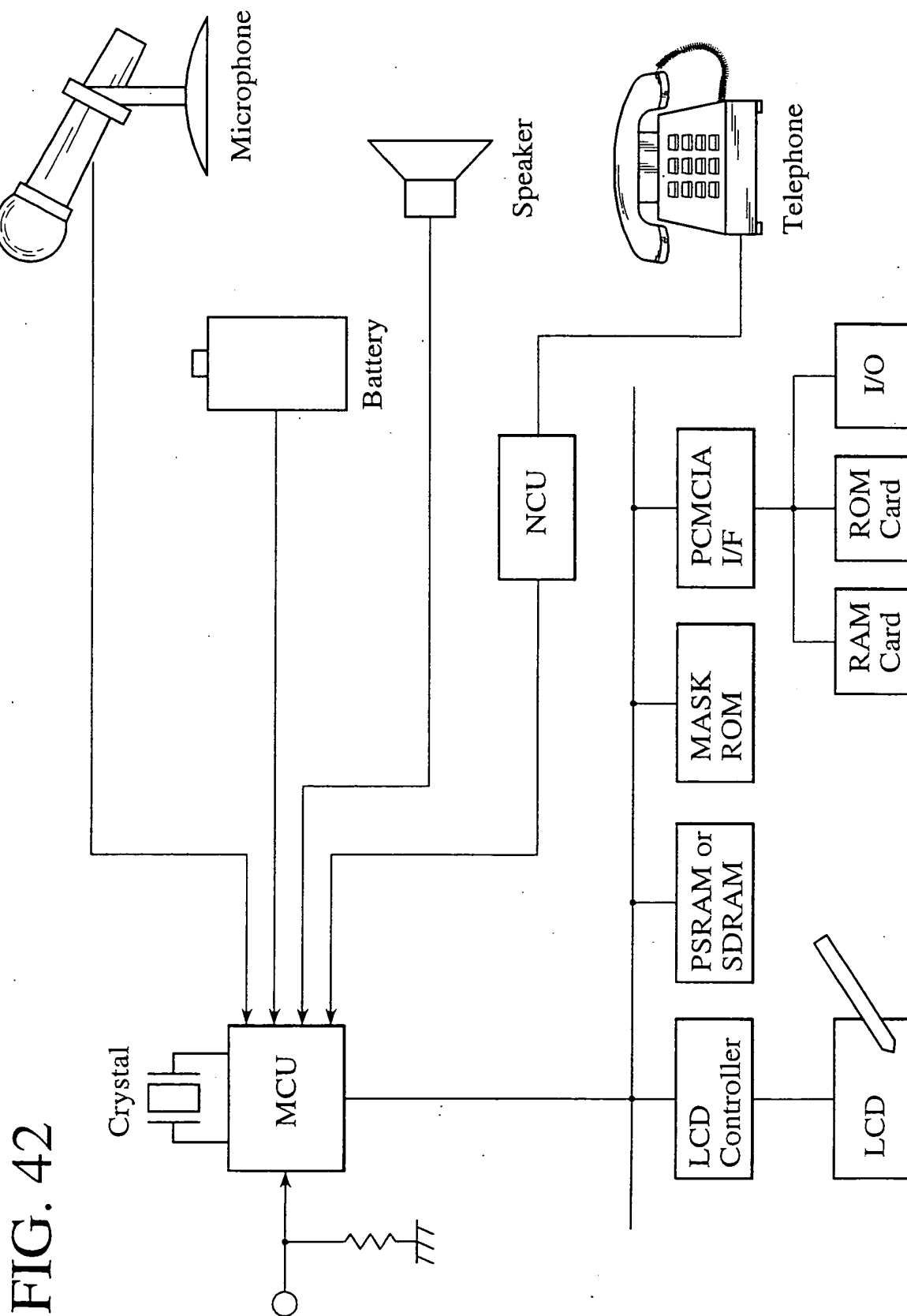


FIG. 42